

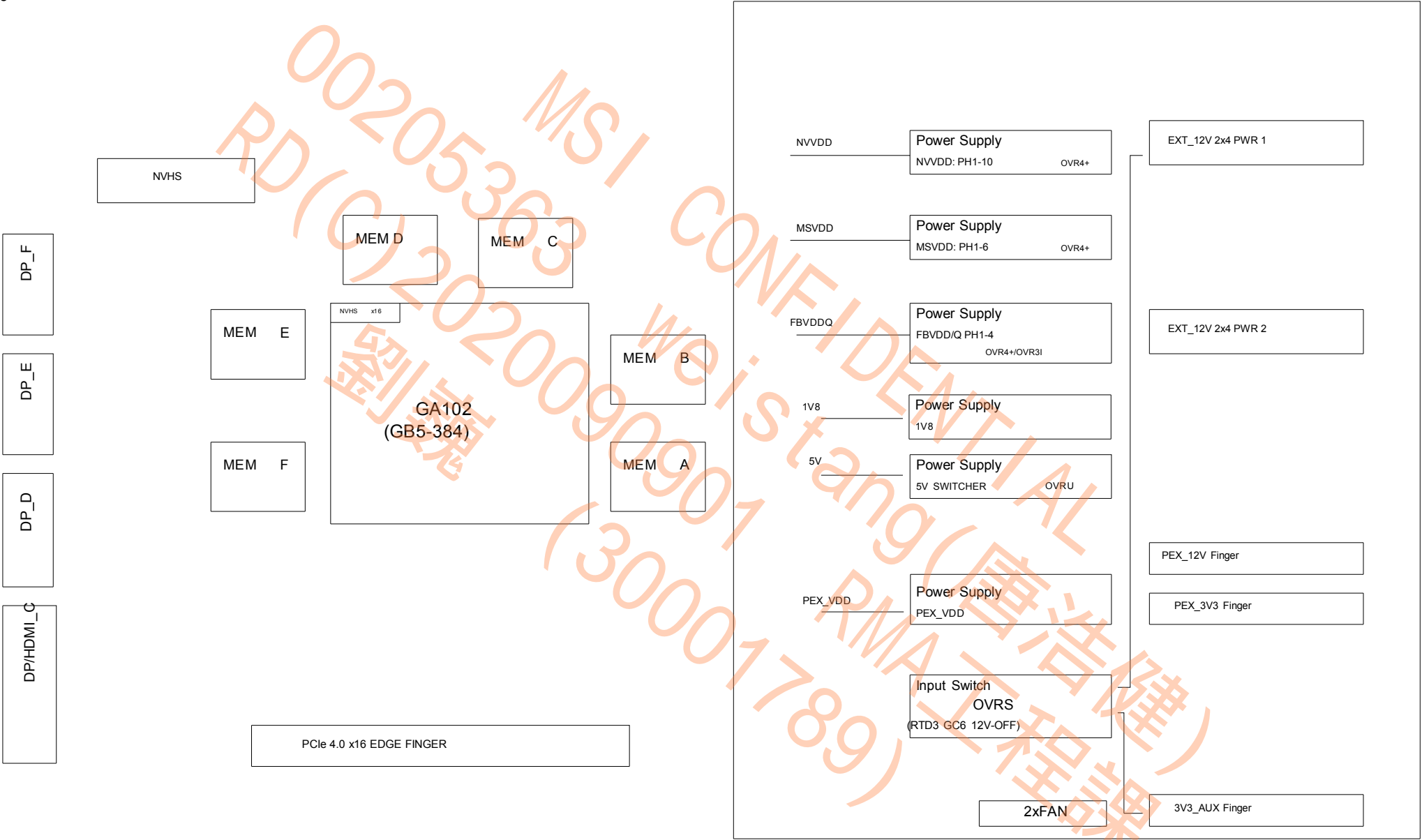
PG132-A02

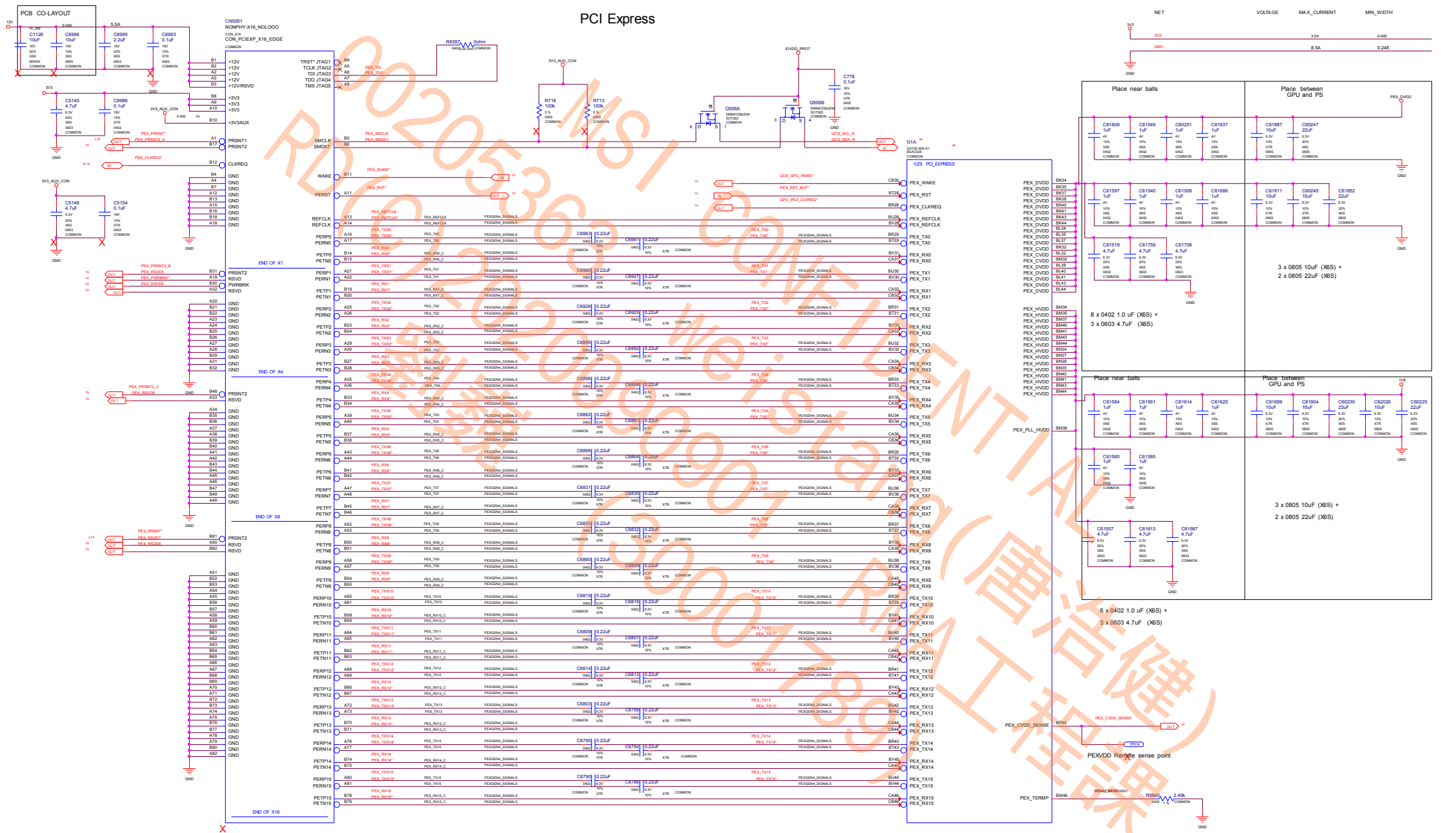
370W, FH Std PCB, 384b, GDDR6x 2CH X16
DP + DP + DP + HDMI/DP

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Block Diagram



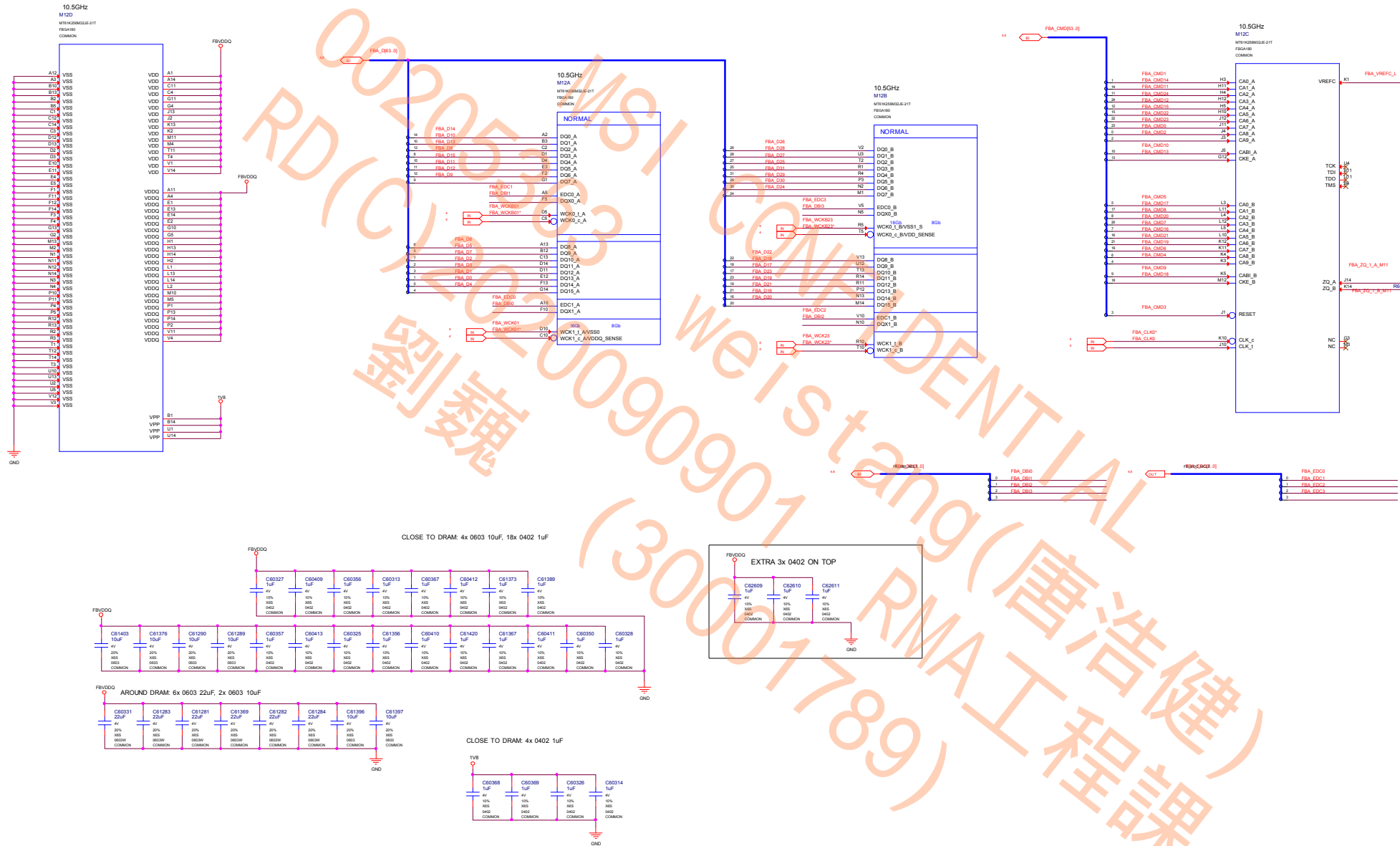


The diagram illustrates the FBUS interface for the G18 and G1C SoCs. It shows the connection of FBUS signals (FBA, FBB, FBA0, FBA1, etc.) to the SoC pins and the internal FBUS controller. The diagram includes a table mapping FBUS signals to SoC pins and a detailed schematic of the FBUS controller and its associated components.

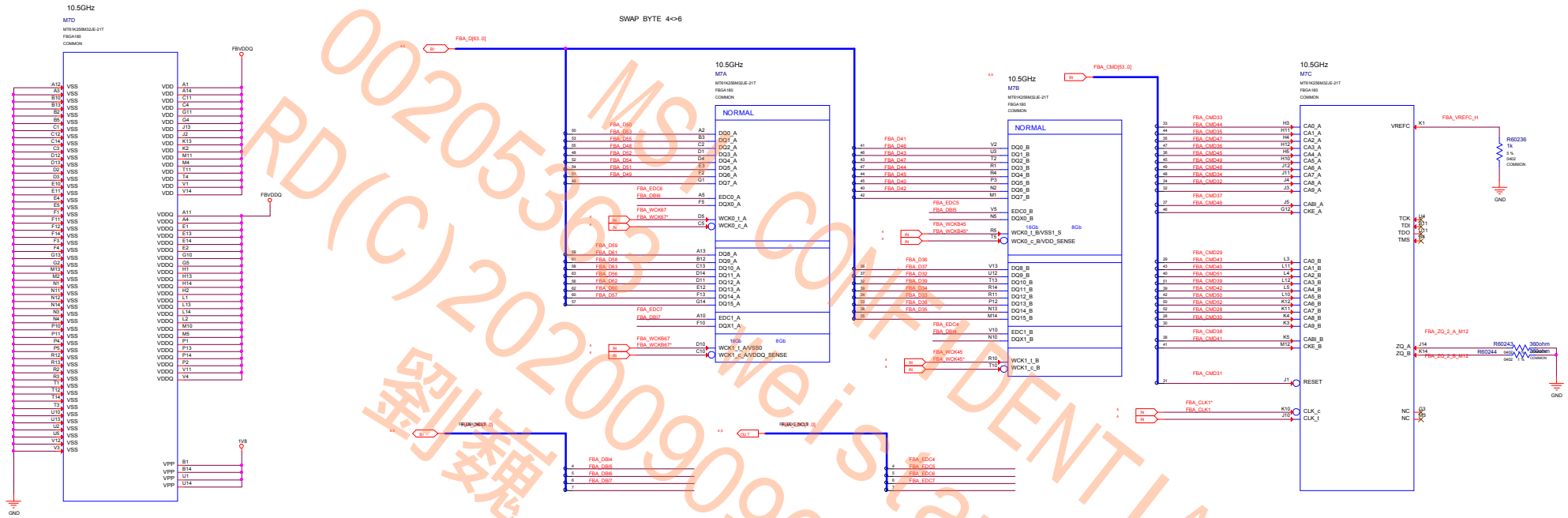
FBUS Signals to SoC Pins Mapping:

FBUS Signal	SoC Pin
FBA_0	FB00
FBA_1	FB01
FBA_2	FB02
FBA_3	FB03
FBA_4	FB04
FBA_5	FB05
FBA_6	FB06
FBA_7	FB07
FBA_8	FB08
FBA_9	FB09
FBA_10	FB10
FBA_11	FB11
FBA_12	FB12
FBA_13	FB13
FBA_14	FB14
FBA_15	FB15
FBA_16	FB16
FBA_17	FB17
FBA_18	FB18
FBA_19	FB19
FBA_20	FB20
FBA_21	FB21
FBA_22	FB22
FBA_23	FB23
FBA_24	FB24
FBA_25	FB25
FBA_26	FB26
FBA_27	FB27
FBA_28	FB28
FBA_29	FB29
FBA_30	FB30
FBA_31	FB31
FBA_32	FB32
FBA_33	FB33
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FBA_102	FB102
FBA_103	FB103
FBA_104	FB104
FBA_105	FB105
FBA_106	FB106
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FBA_123	FB123
FBA_124	FB124
FBA_125	FB125
FBA_126	FB126
FBA_127	FB127
FBA_128	FB128
FBA_129	FB129
FBA_130	FB130
FBA_131	FB131
FBA_132	FB132
FBA_133	FB133
FBA_134	FB134
FBA_135	FB135
FBA_136	FB136
FBA_137	FB137
FBA_138	FB138
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FBA_142	FB142
FBA_143	FB143
FBA_144	FB144
FBA	

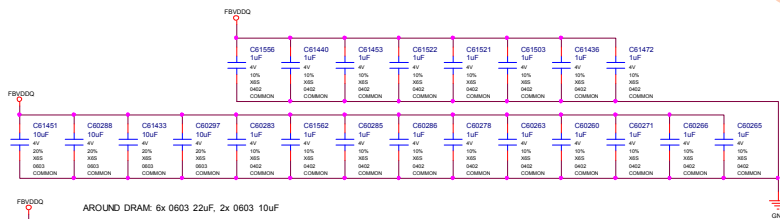
MEMORY: FBA Partition 31..0



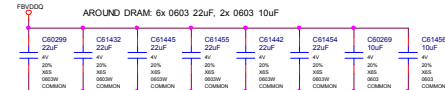
MEMORY: FBA Partition 63..32



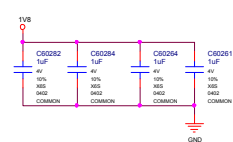
CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF



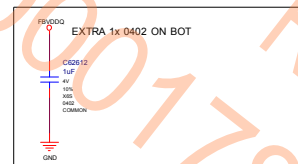
AROUND DRAM: 6x 0603 22uF, 2x 0603 10uF



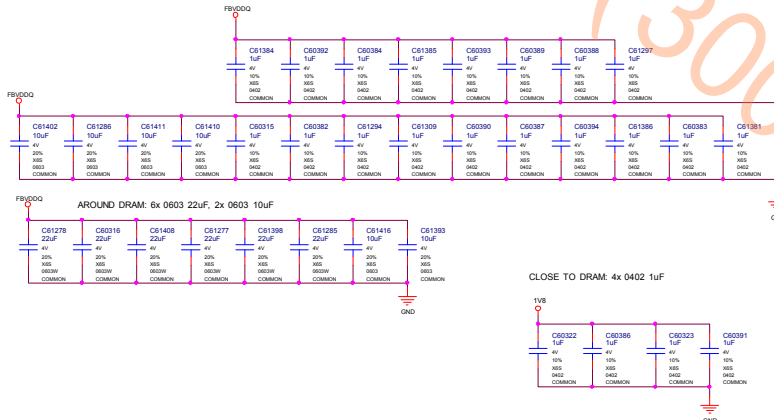
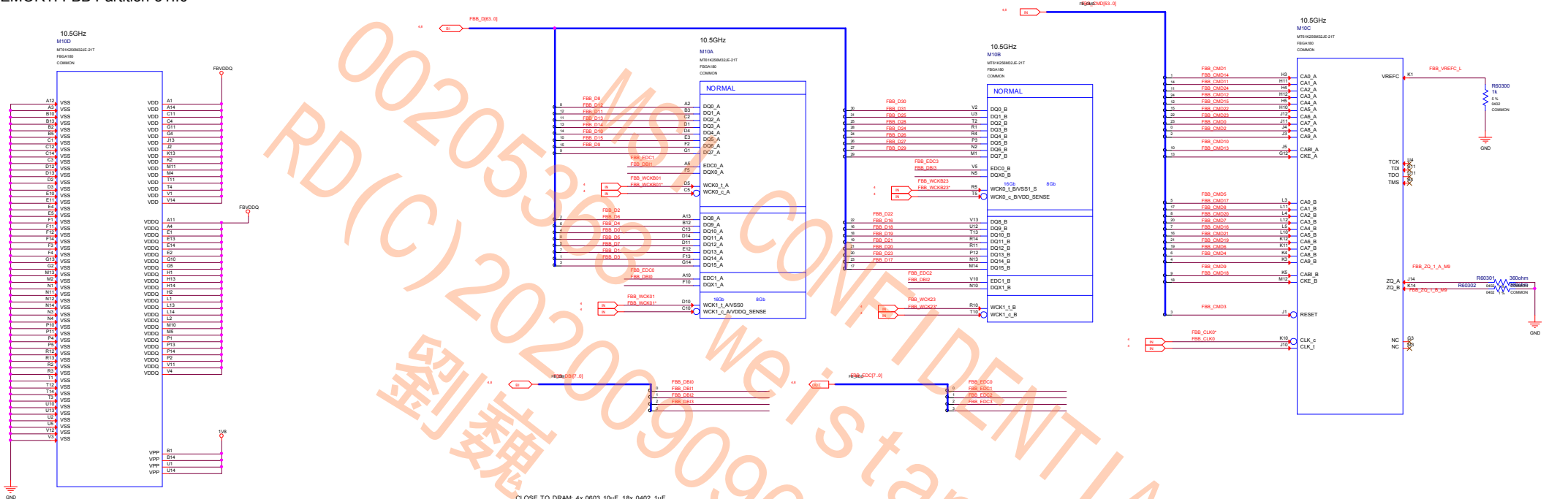
CLOSE TO DRAM: 4x 0402 1uF



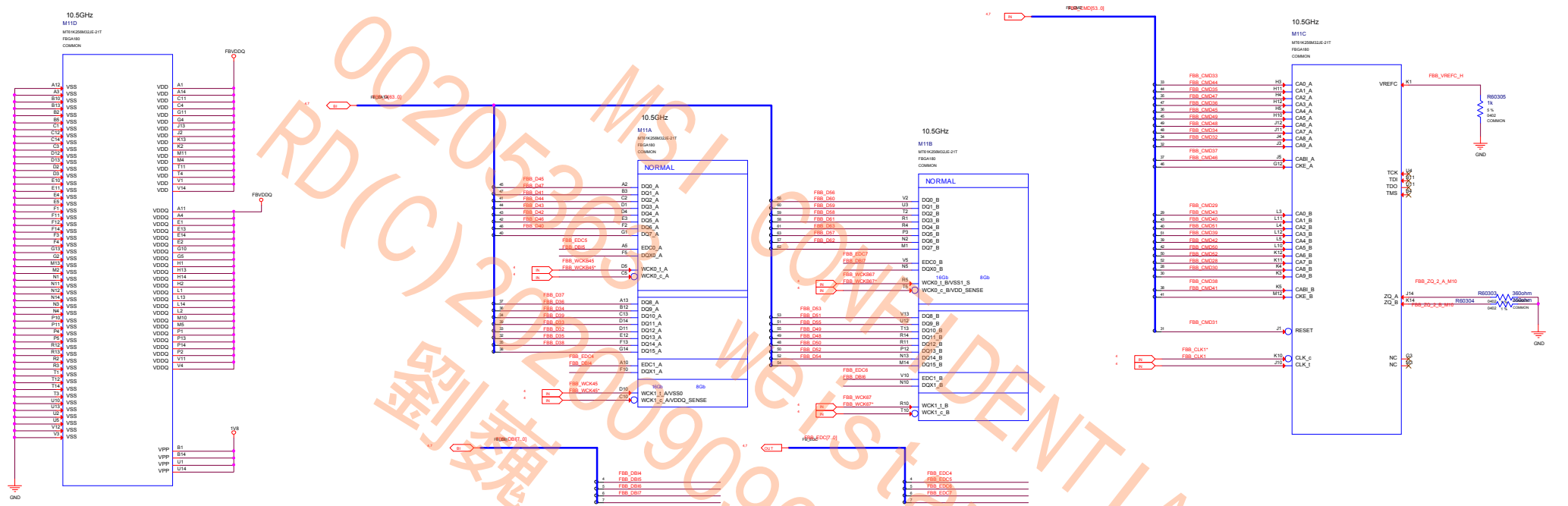
FBYDDQ EXTRA 1x 0402 ON BOT



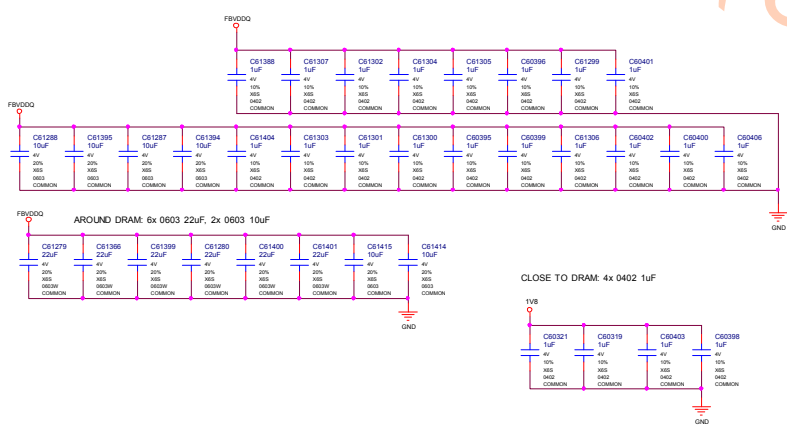
MEMORY: FBB Partition 31..0



MEMORY: FBB Partition 63..32

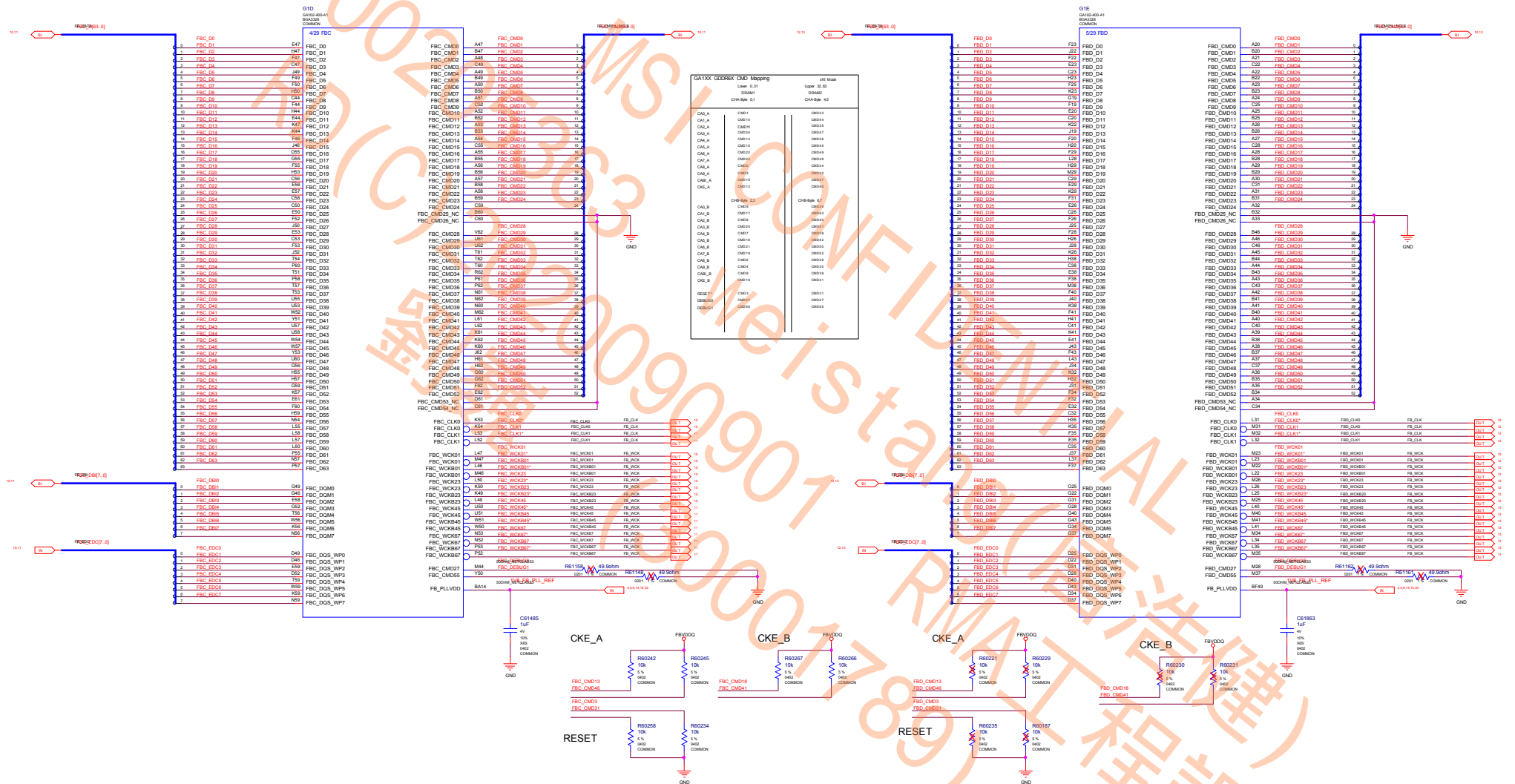


CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF

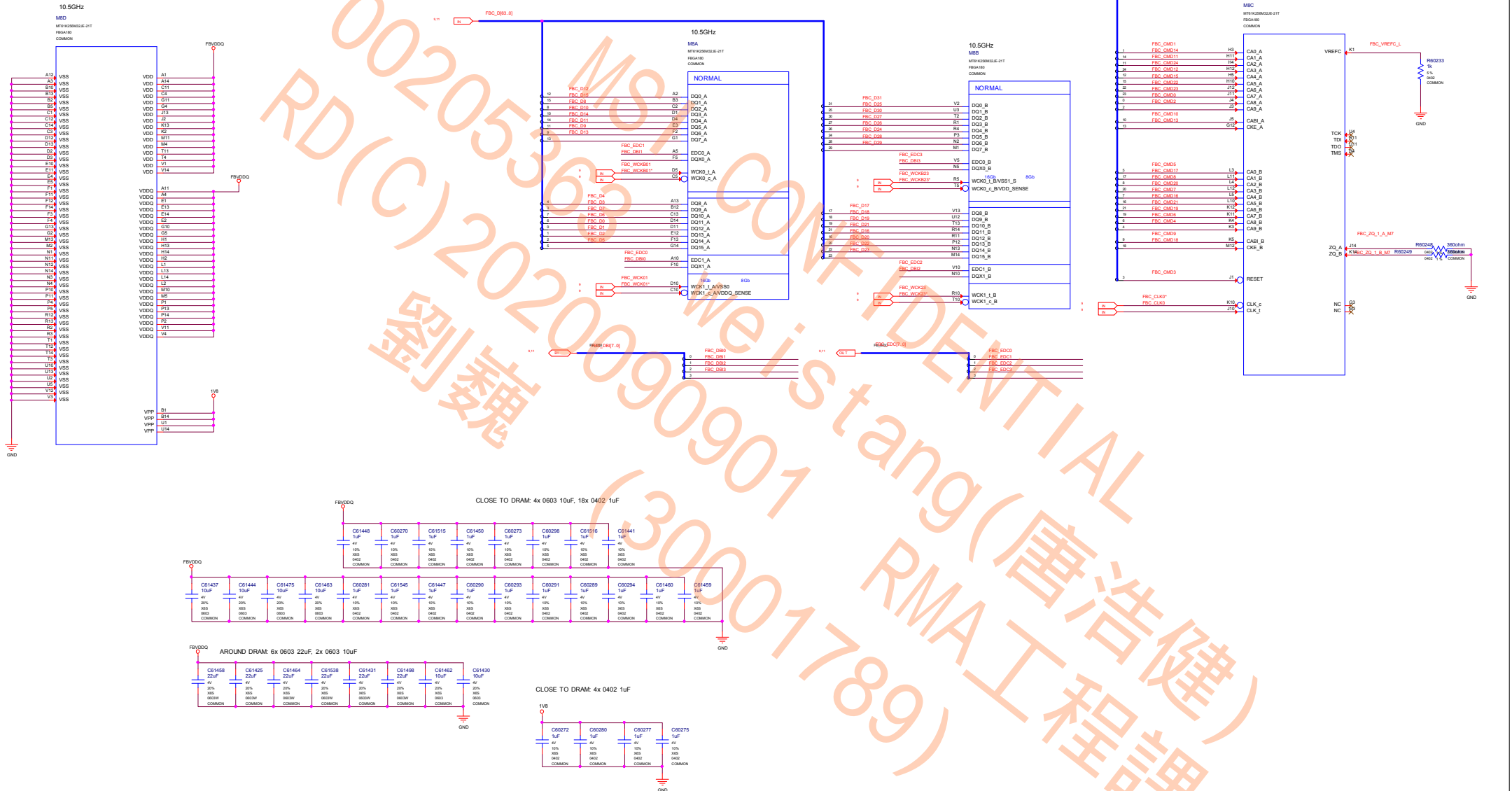


CLOSE TO DRAM: 4x 0402 1uF

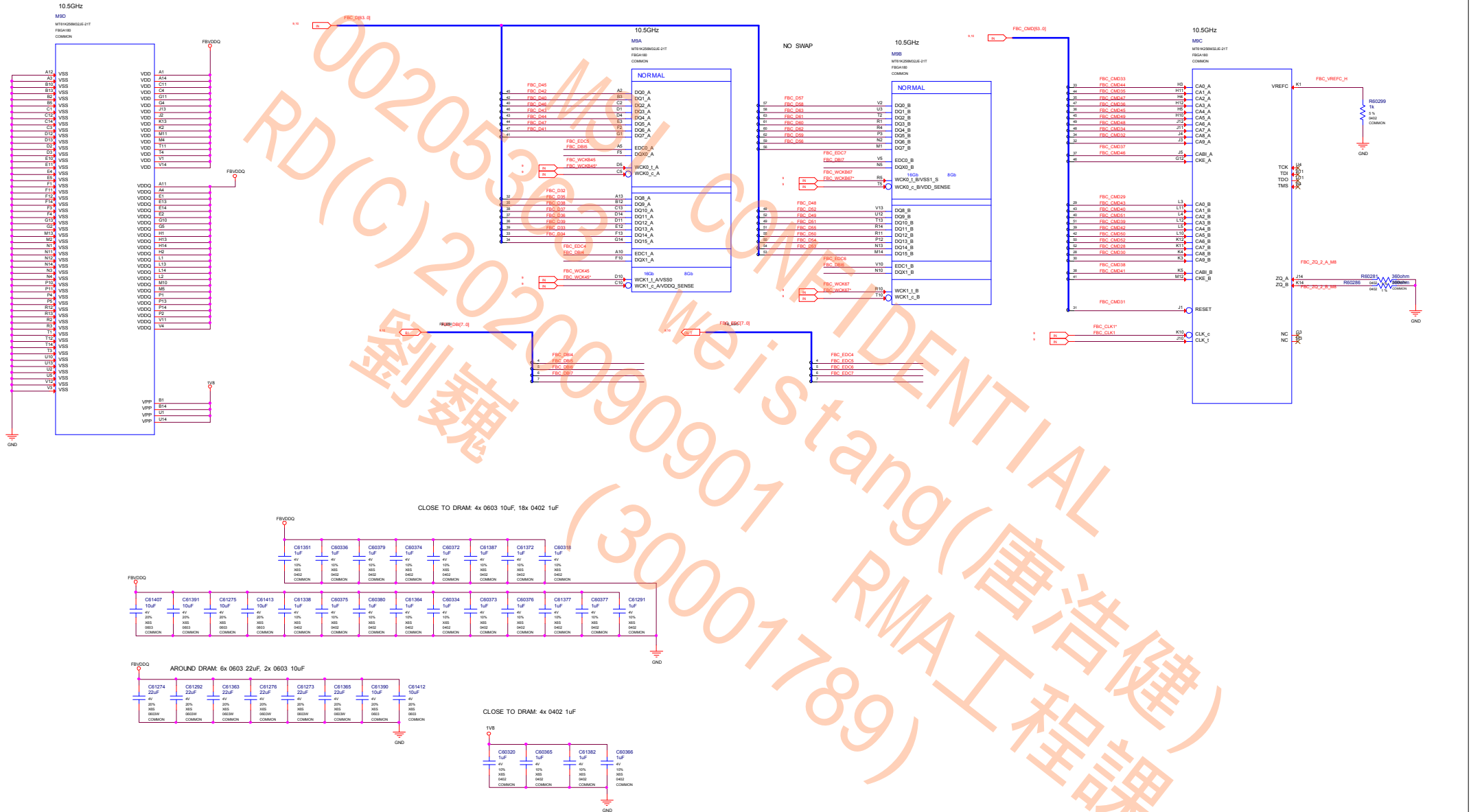
MEMORY: GPU Partition C/D



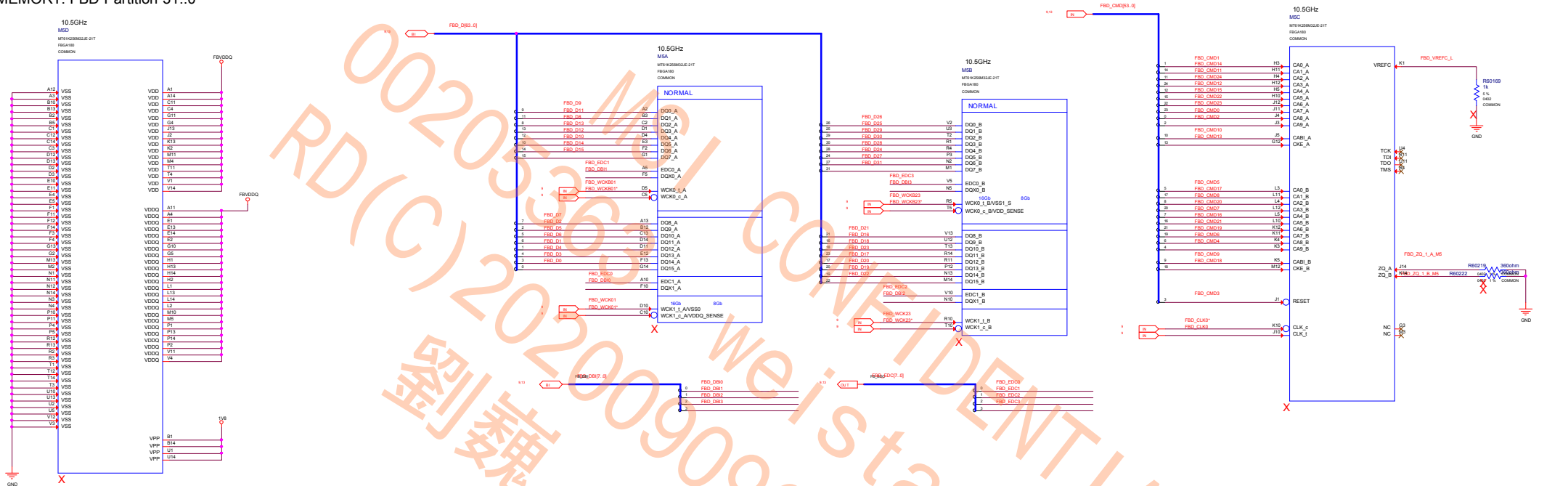
MEMORY: FBC Partition 31..0



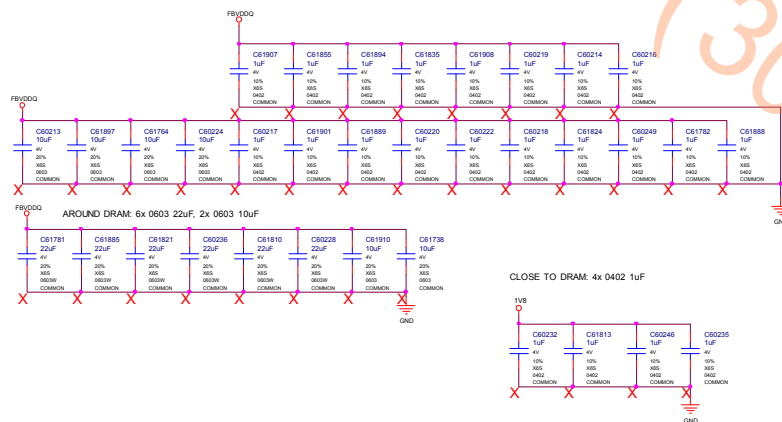
MEMORY: FBC Partition 63..32



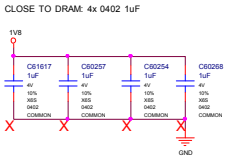
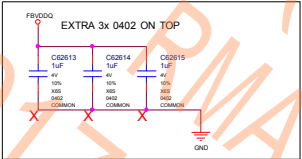
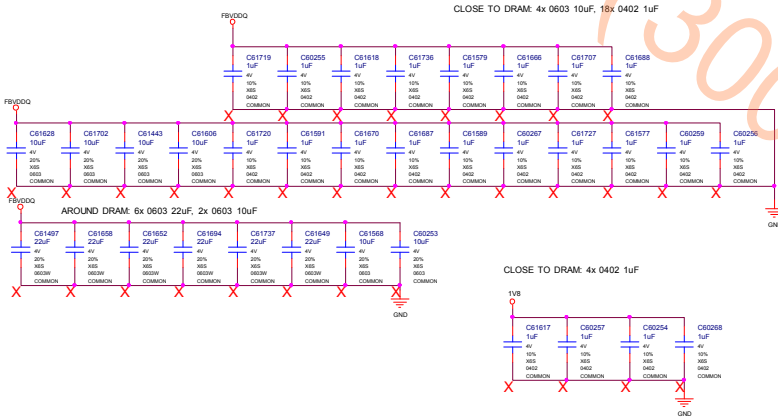
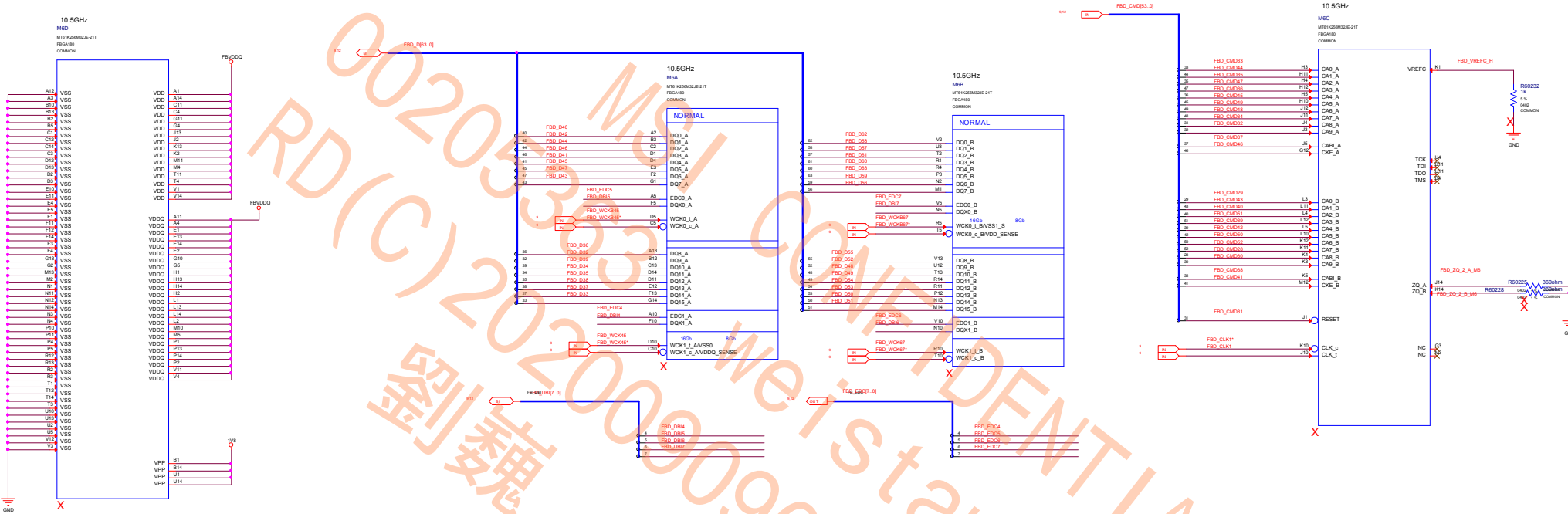
MEMORY: FBD Partition 31..0



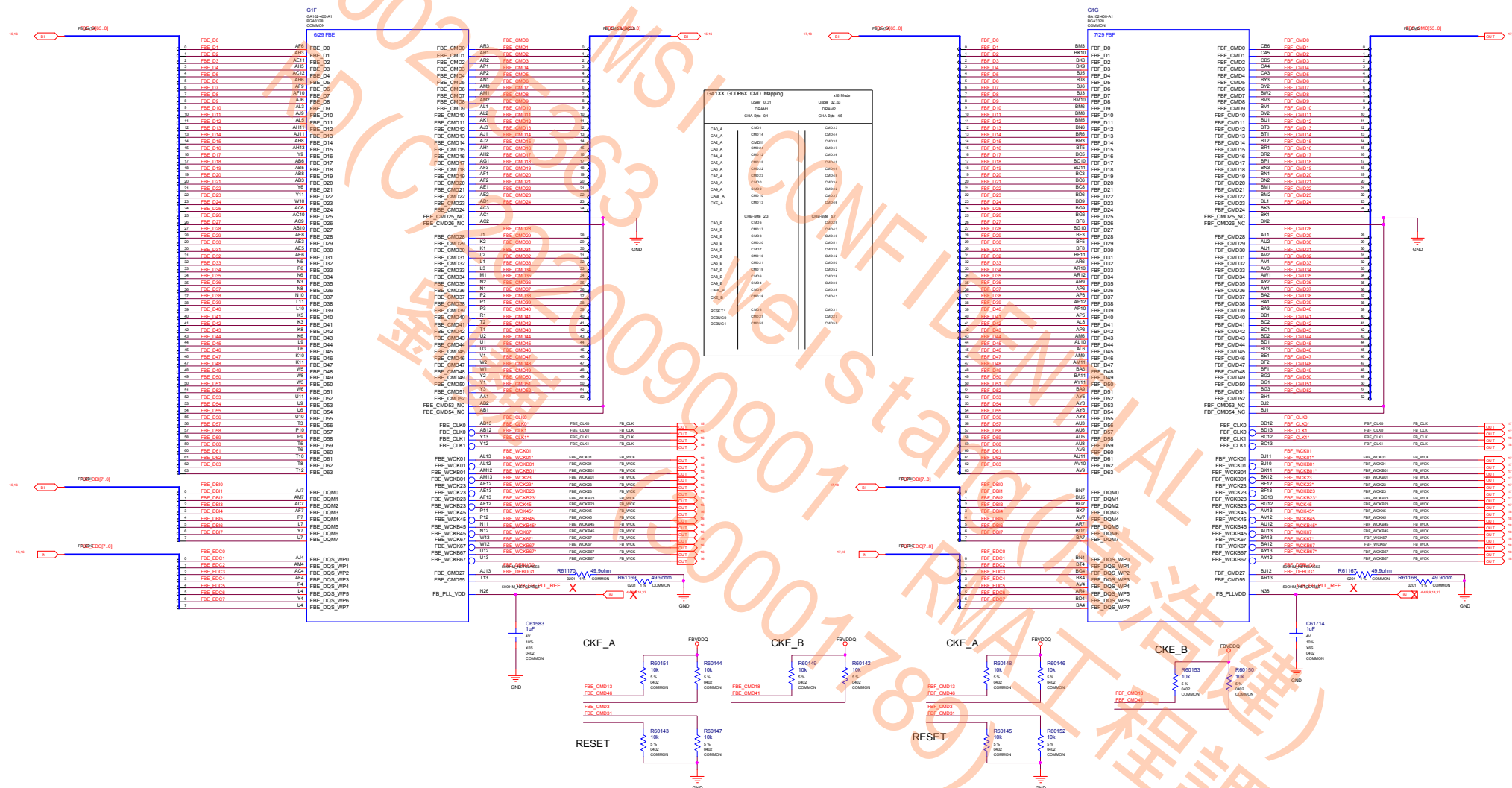
CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF



MEMORY: FBD Partition 63..32



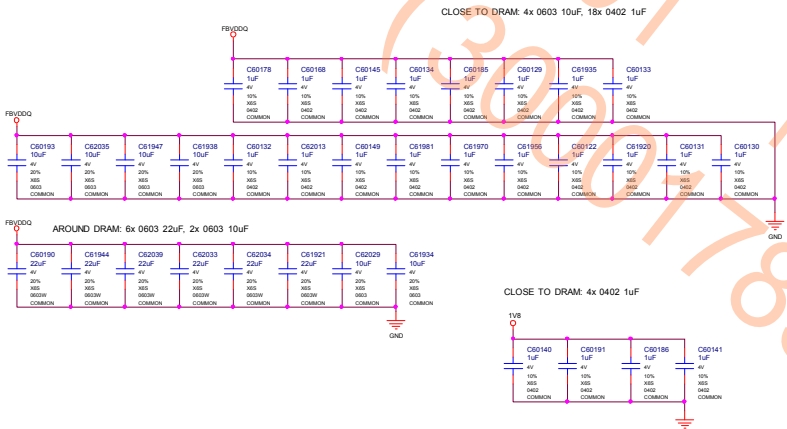
MEMORY: GPU Partition E/F

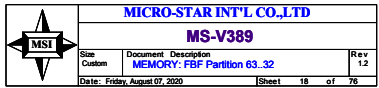


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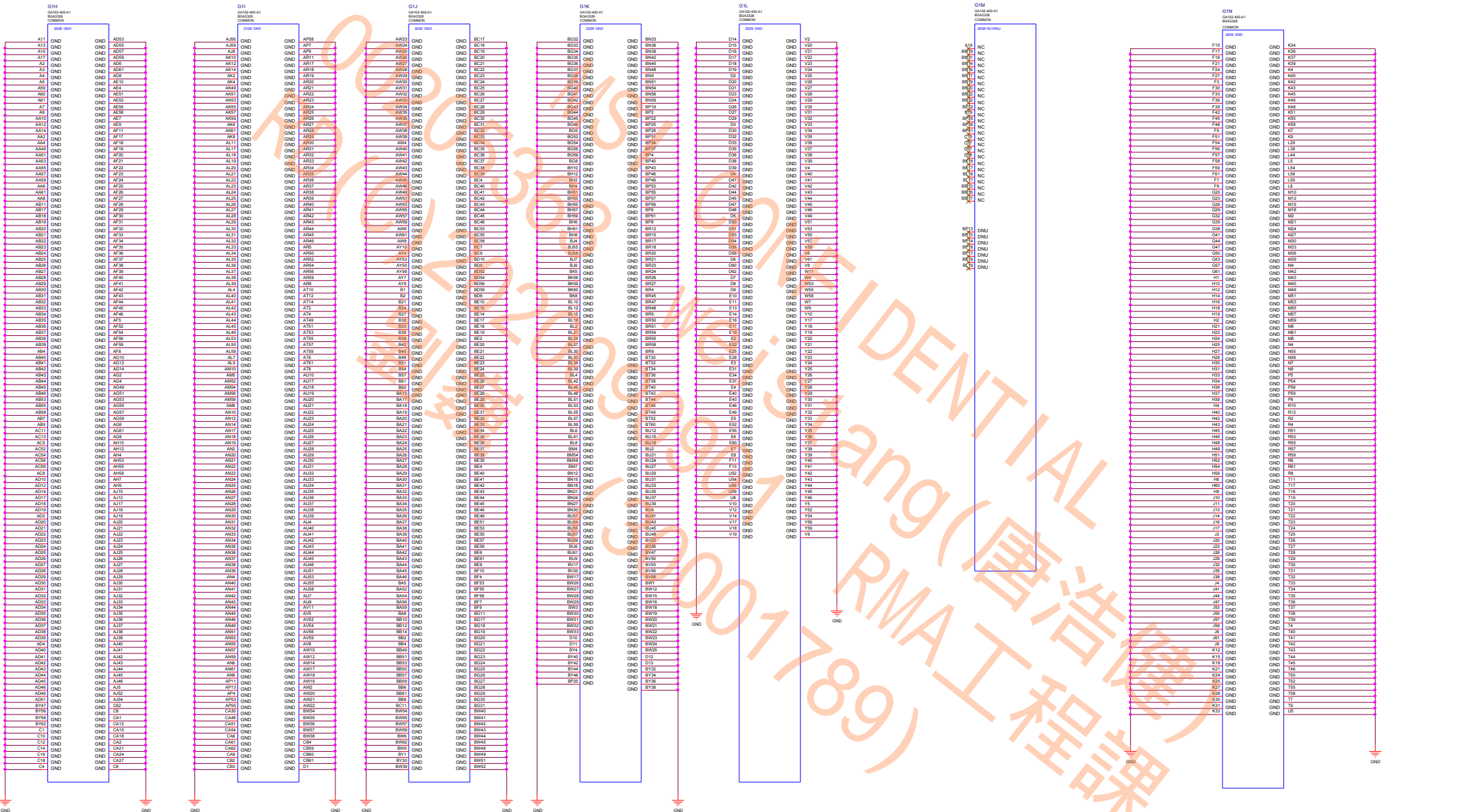
MEMORY: FBE Partition 63..32



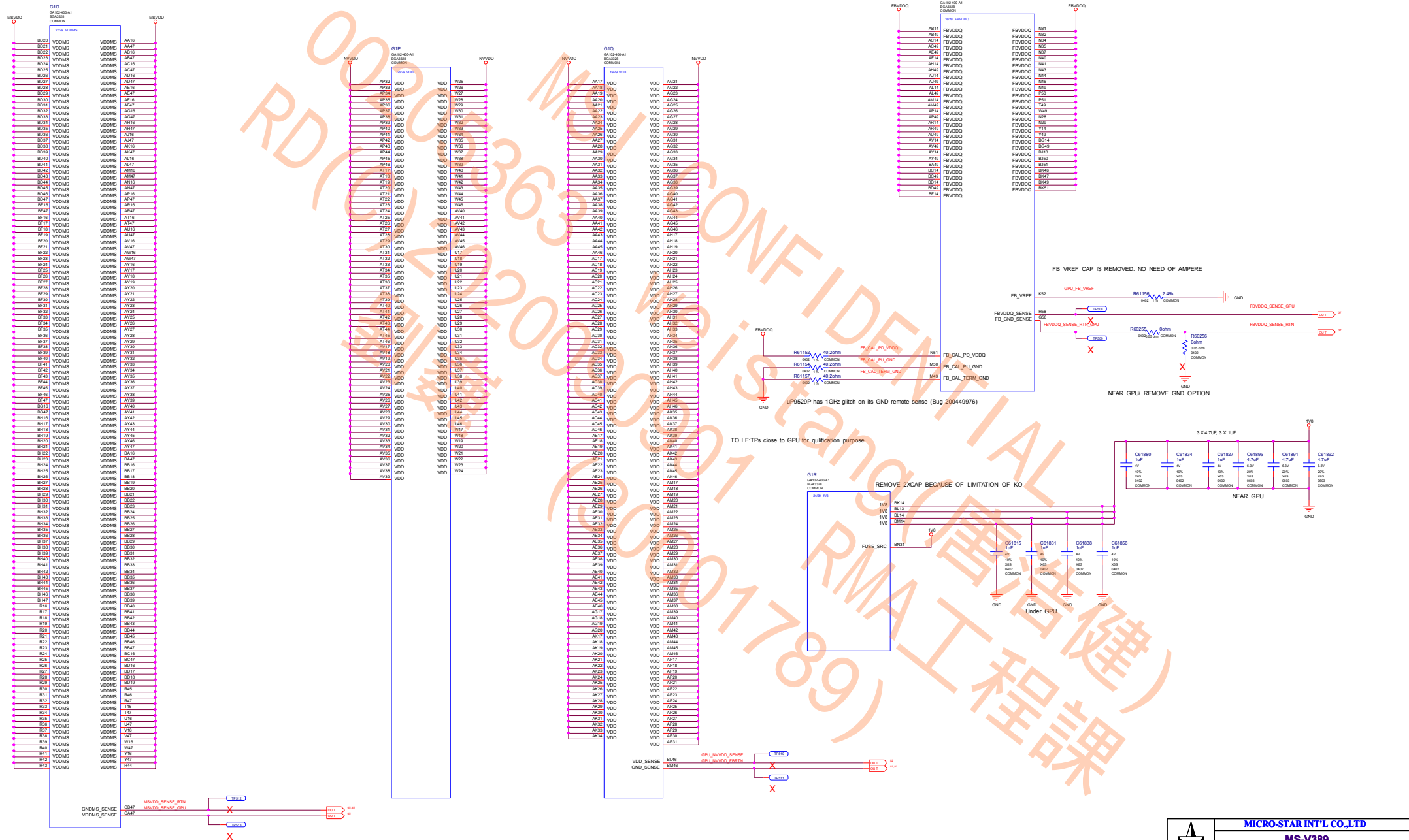


[illegible]

GPU GND, RFUs & RSVD

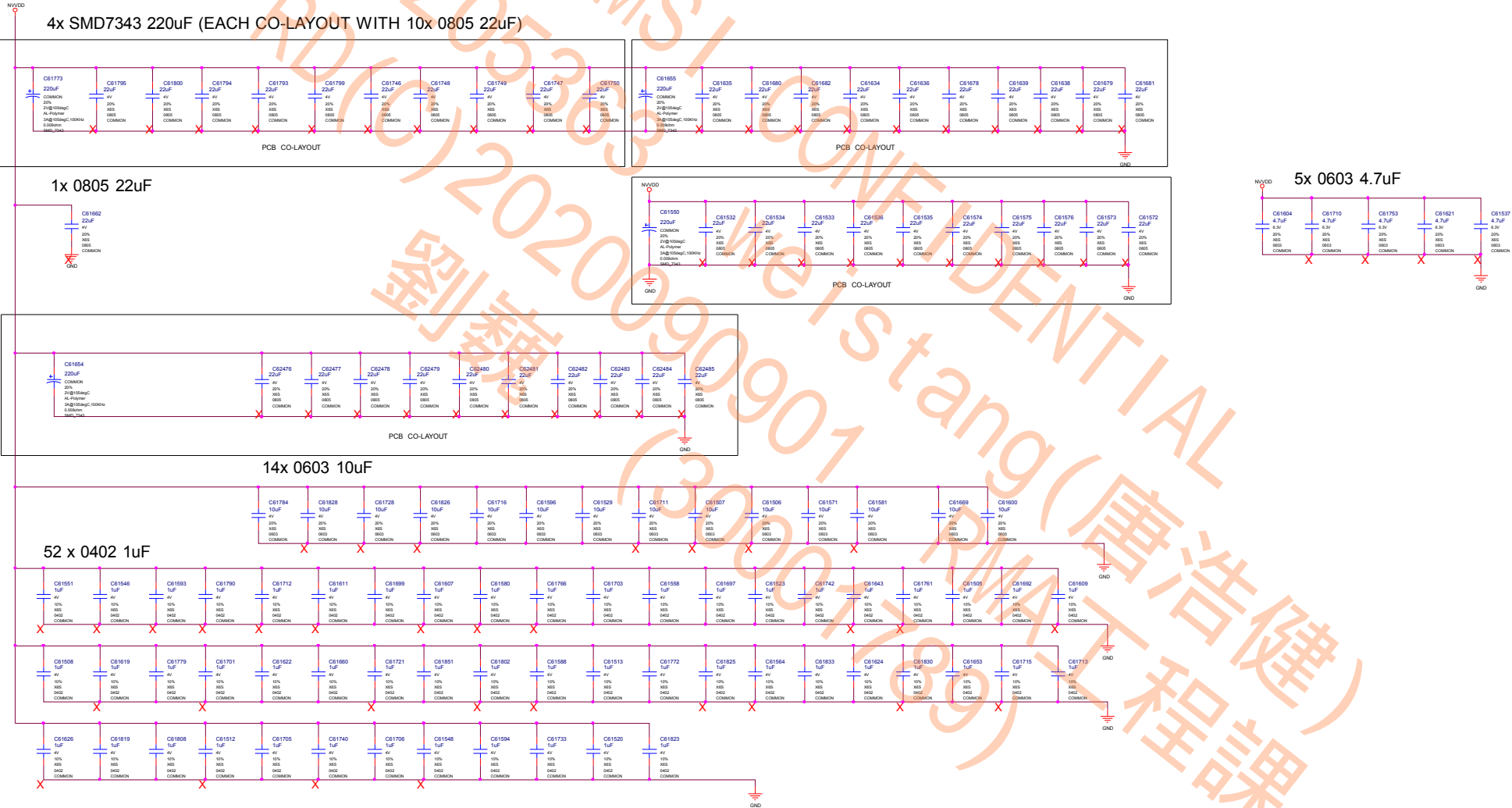


GPU PWR and GND

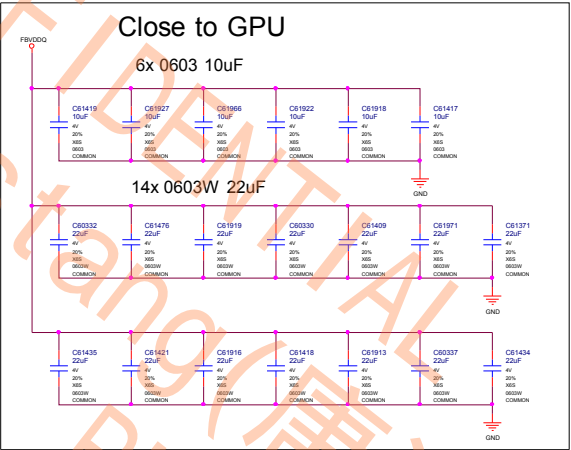


NVVDD

UNDER GPU

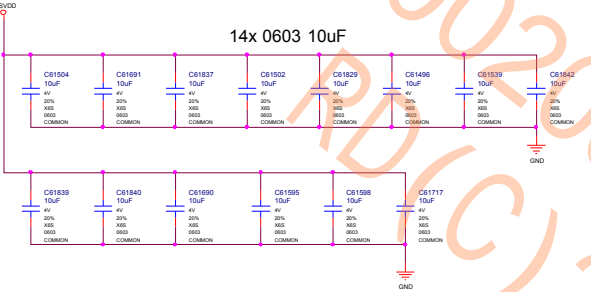


FBVDDQ

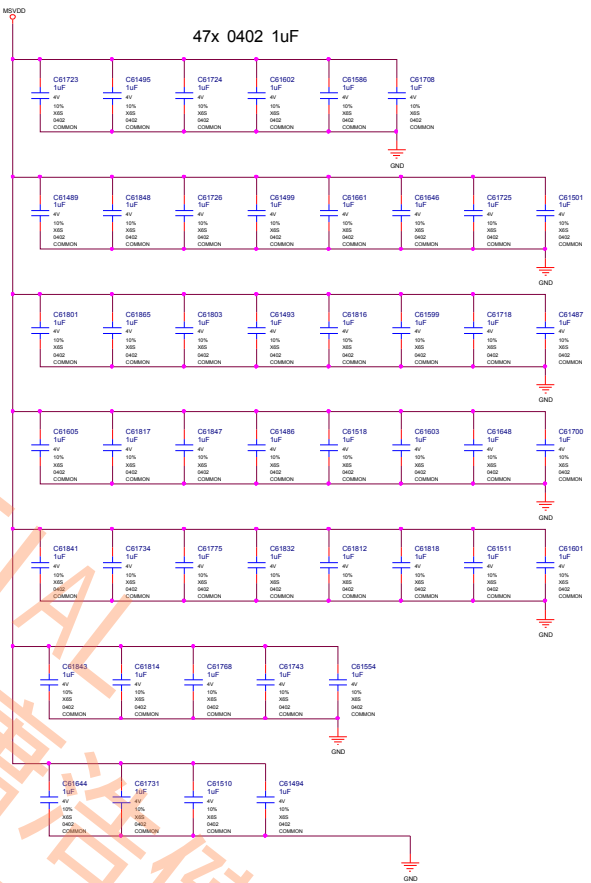
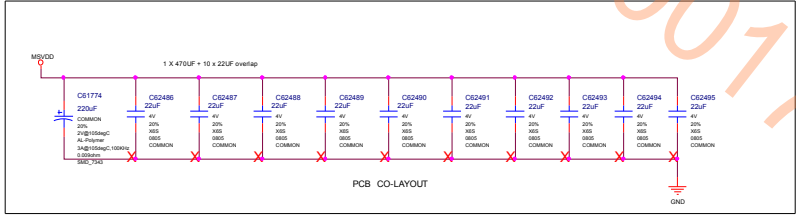
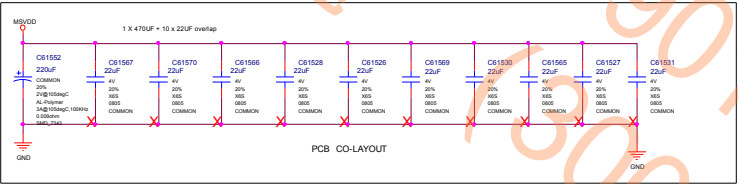


UNDER GPU

MSVDD



2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION

MSI CONFIDENTIAL
00205363
RD(C)2020090901
Weistang (唐浩健)
RMA工程課
(30001789)

BLANK

NEAR GPU

Capacitor	Value	Notes
C80169	22uF	10% 0805 COMMON
C80392	22uF	10% 0805 COMMON
C80160	6.3V 10uF	10% 0805 COMMON
C80173	6.3V 10uF	10% 0805 COMMON
C80175	6.3V 10uF	10% 0805 COMMON
C81797	4.7uF	20% 0805 COMMON
C81798	4.7uF	20% 0805 COMMON
C81763	4.7uF	20% 0805 COMMON
C81876	1uF	10% 0805 COMMON
C81780	1uF	10% 0805 COMMON
C81678	1uF	10% 0805 COMMON
C81732	1uF	10% 0805 COMMON
C81776	1uF	10% 0805 COMMON
C81741	1uF	10% 0805 COMMON
C81777	1uF	10% 0805 COMMON

UNDER GPU

REMOVE ONE BECAUSE OF KO LIMITATION

BRIDGE POR

LED -> NO

ID ROM -> YES

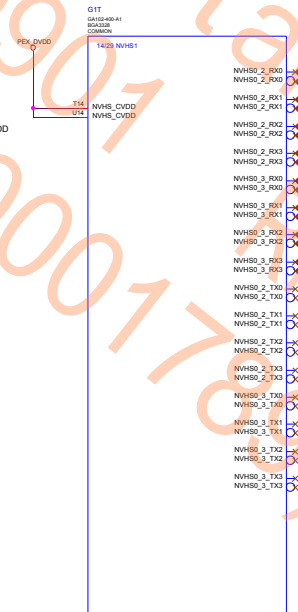
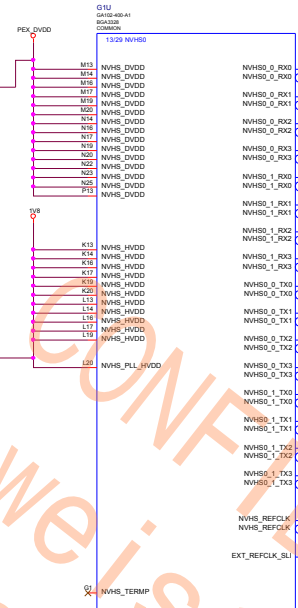
NEAR GPU

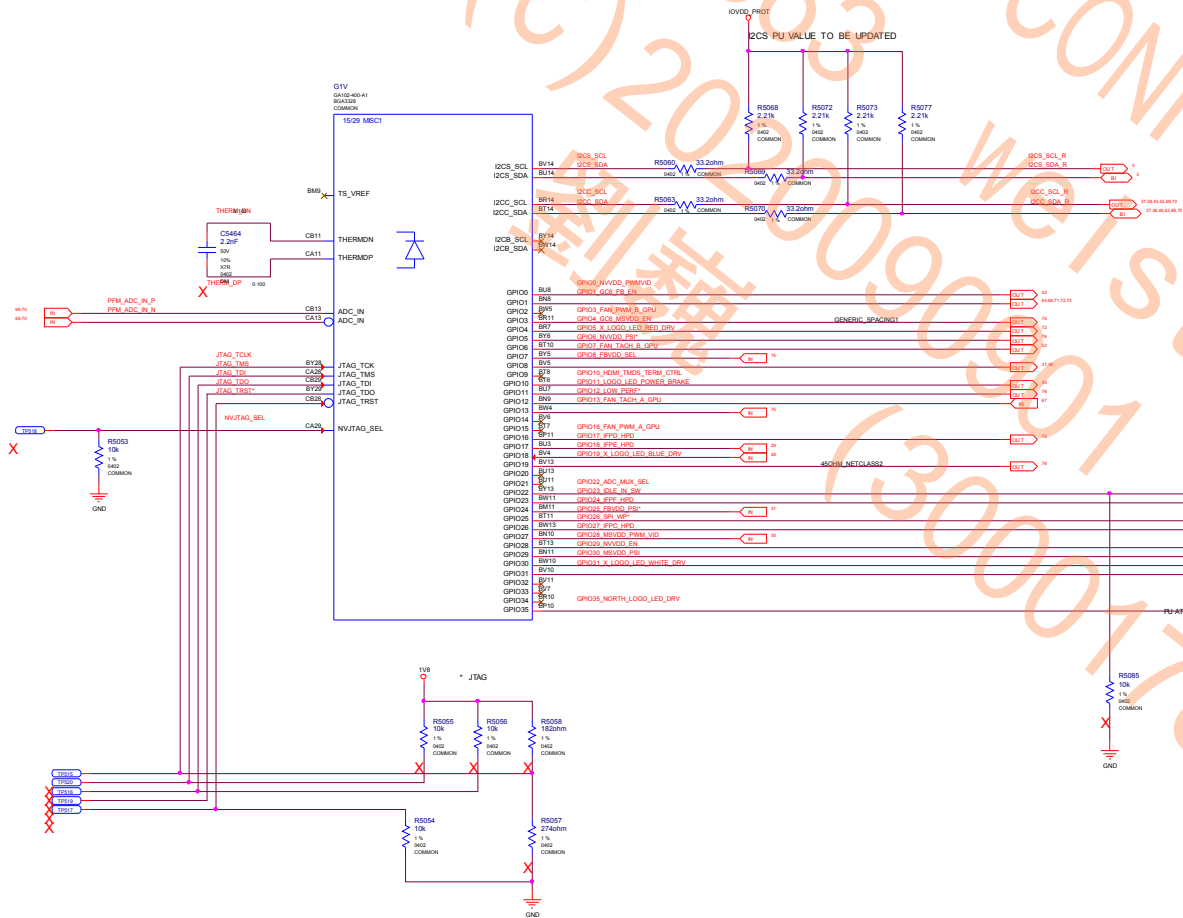
Capacitor	Value	Notes
C81905	10uF	10% 0805 COMMON
C81877	4.7uF	20% 0805 COMMON
C81822	4.7uF	20% 0805 COMMON
C81820	4.7uF	20% 0805 COMMON
C81807	1uF	10% 0805 COMMON
C81857	1uF	10% 0805 COMMON
C81806	1uF	10% 0805 COMMON
C81845	1uF	10% 0805 COMMON
C81846	1uF	10% 0805 COMMON
C81844	1uF	10% 0805 COMMON

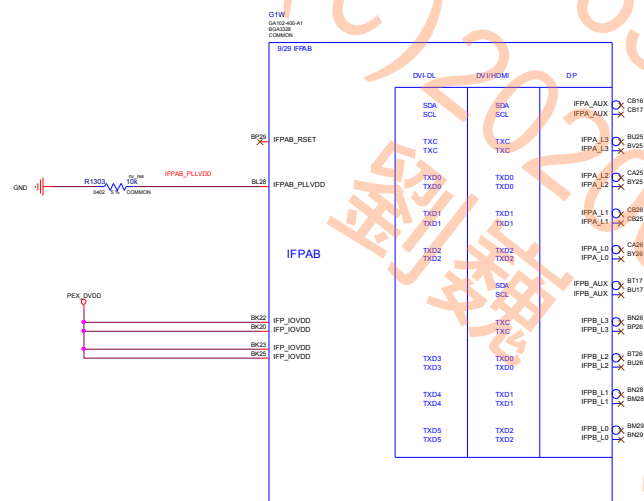
UNDER GPU

REMOVE ONE BECAUSE OF KO LIMITATION

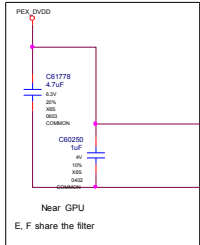
REMOVED 4x 0805
TO OPTIMIZE FBVDDQ PLANE

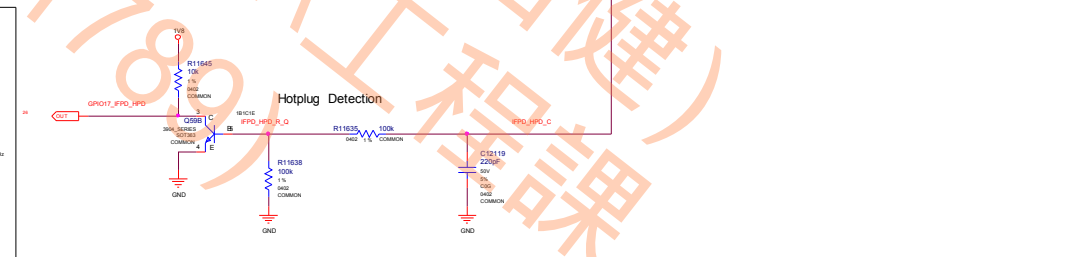
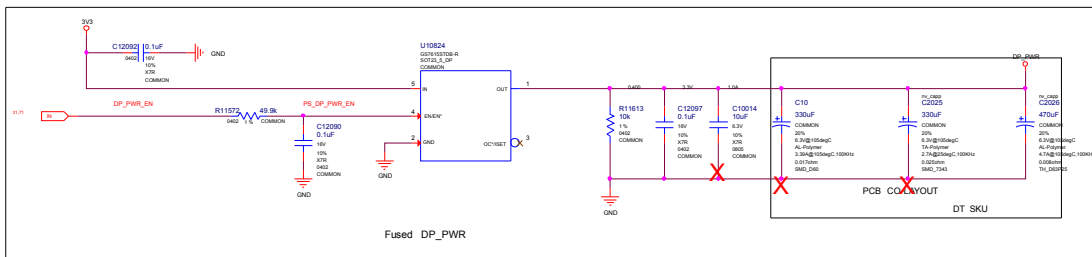
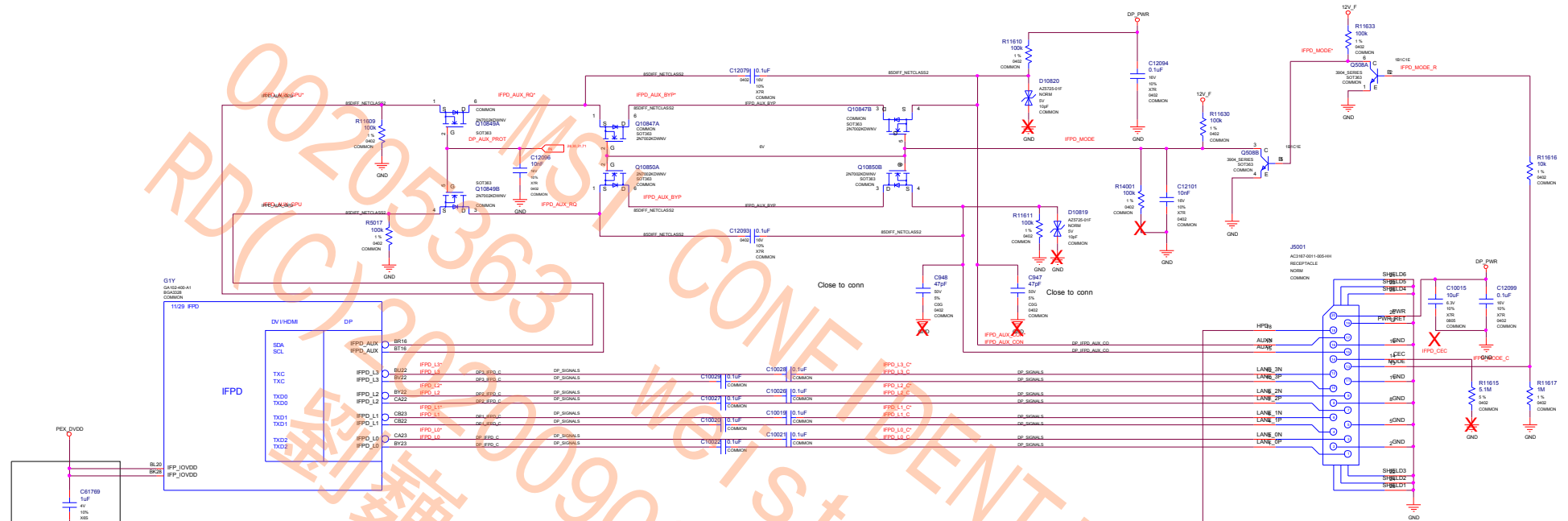




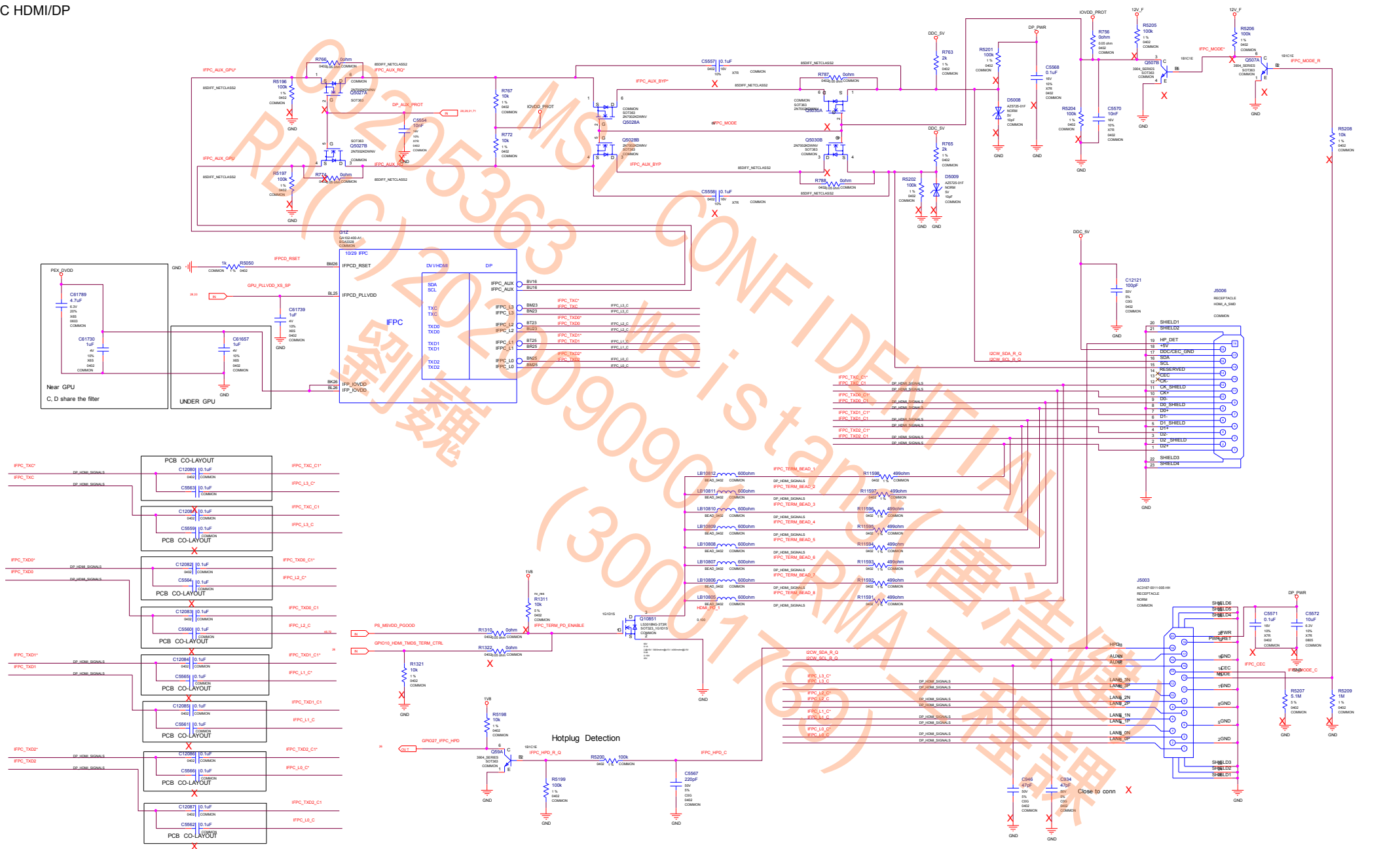
[illegible]

IFPE DP





IFPC HDMI/DP



MISC: ROM, Straps

GROUP0	STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
	L	L	L	00000	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)
	H	L	L	00100	RAMCFG MICRON 8Gb G6X 19Gbps x8 (161-0430-900)
	H	L	H	00101	RAMCFG MICRON 8Gb G6X 21Gbps x8 (161-0431-900)
	L	L	M	01000	RAMCFG MICRON 8Gb G6X 20Gbps x16 (161-0424-900)
	L	L	H	00001	RAMCFG MICRON 8Gb G6X 21Gbps x16 (161-0431-900)
	L	M	H	01010	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0].FS_OVERT	1:ENABLE 0:DISABLE	DEFAULT
H	H	H	0111	FS_OVERT ENABLE	
L	L	L	0000	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	
L	L	L	0	0	0	0	

Default

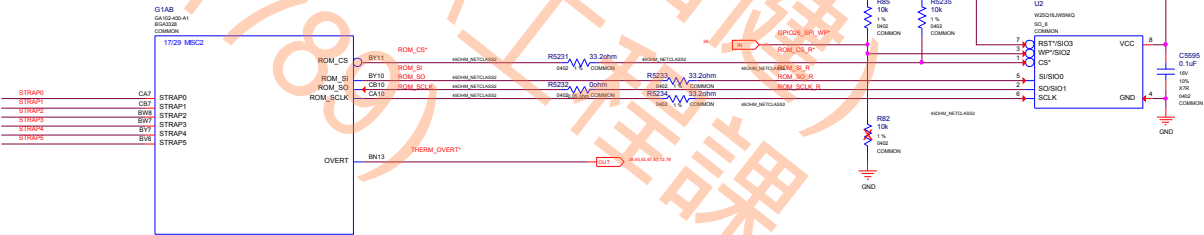
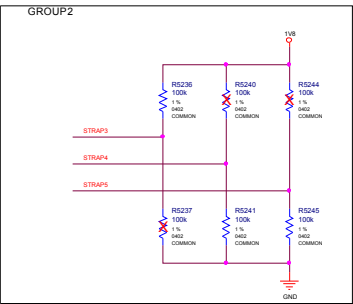
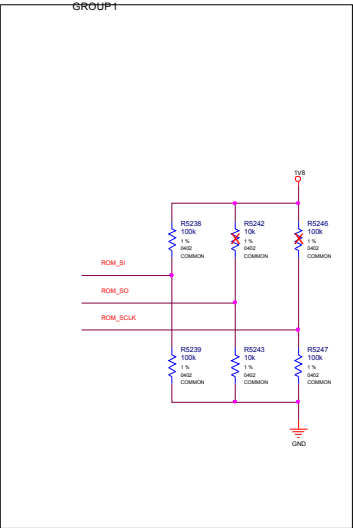
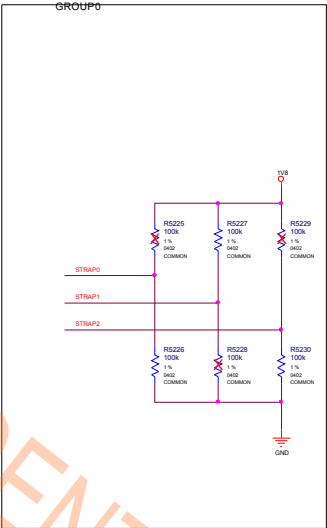
Default

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

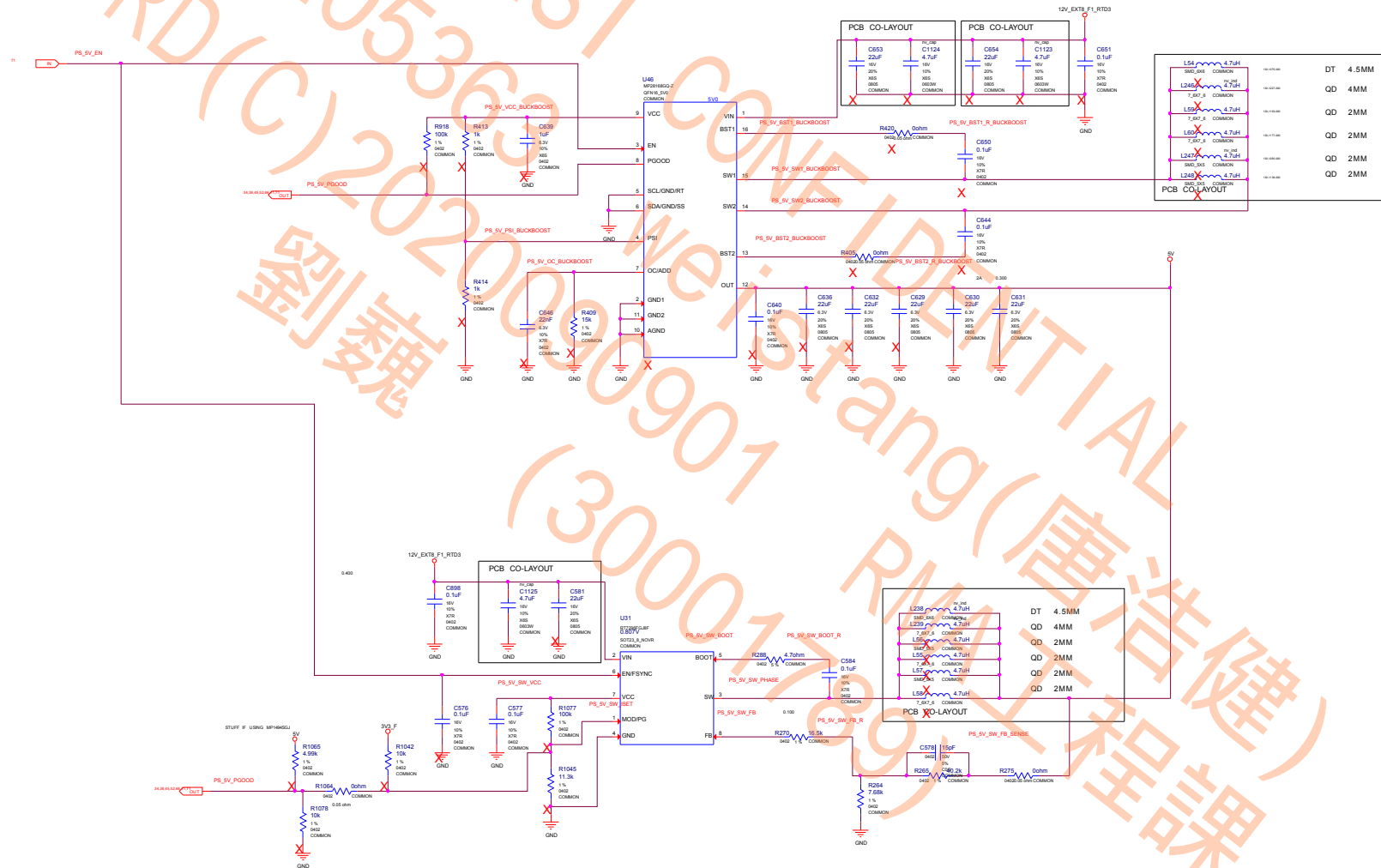
<A01 PCB

<OLD

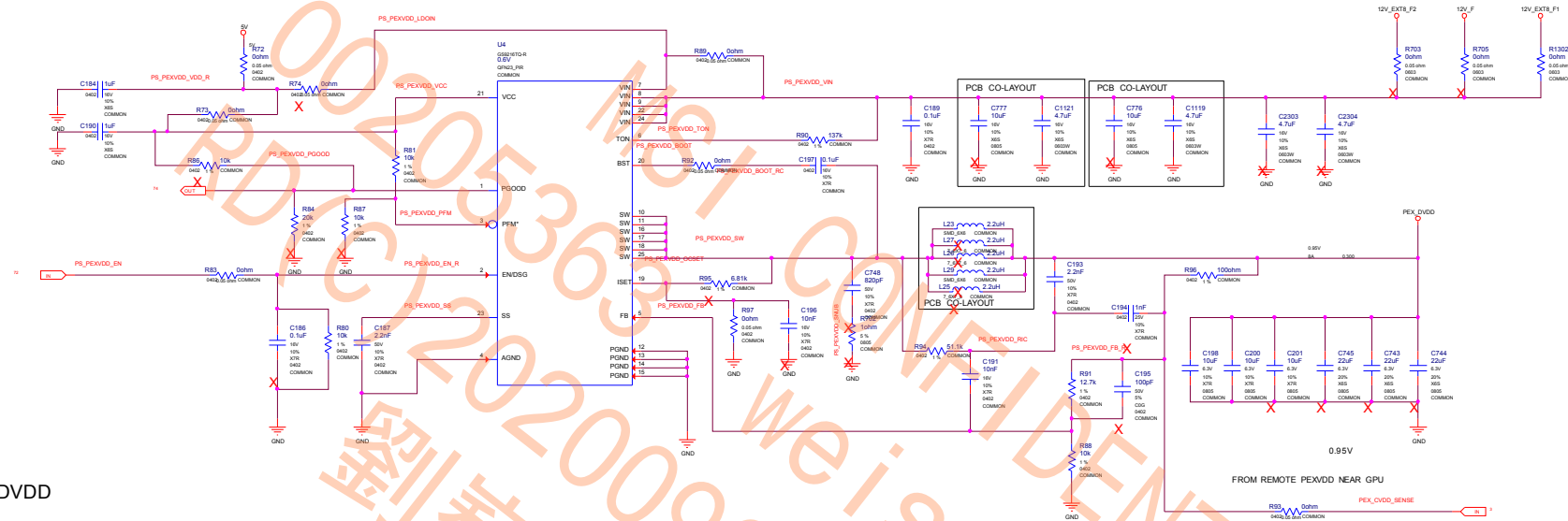
<LATEST A02 PCB



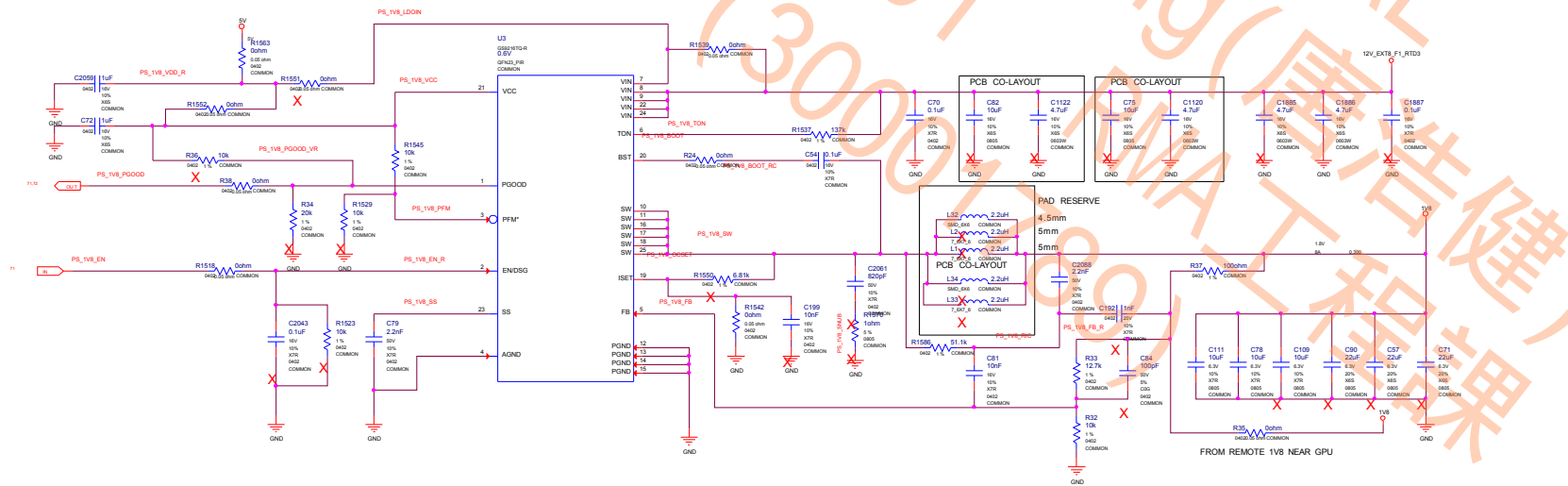
PS: 5V, 5V_BACKUP



PS: PEX_DVDD 1V8 Rail



PEX_DVDD



1V8

00205363 MS/ CONFIDENTIAL
RD(C)2020-0901 Weistang (唐浩健)
BLANK (30001789) RMA工程課

PIN12 MP2988 VIN SENSE 1/16 DIVIDER
PIN12 UP9529 REFOUT





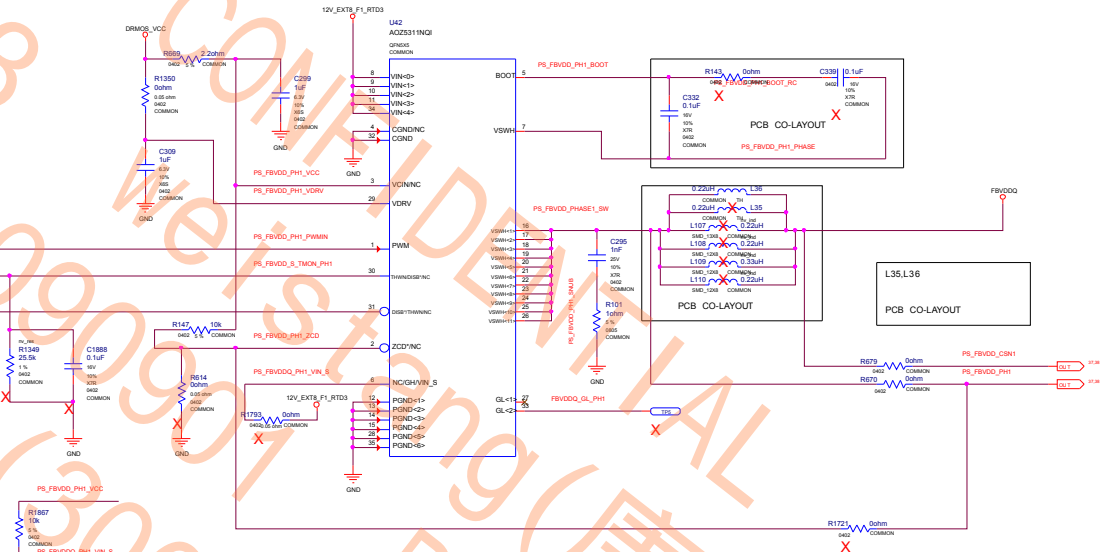
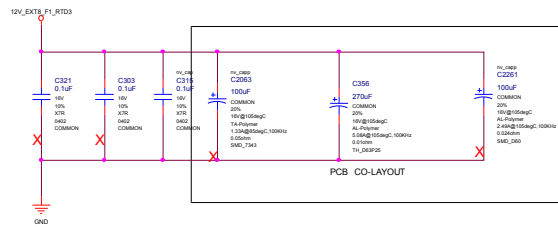
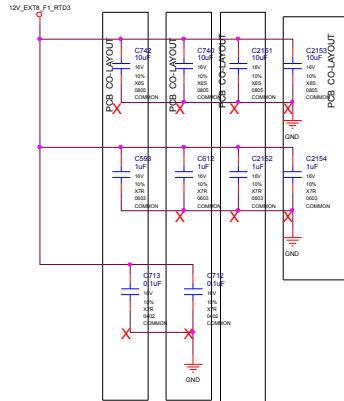
UP9512

N. AND IN 05/94

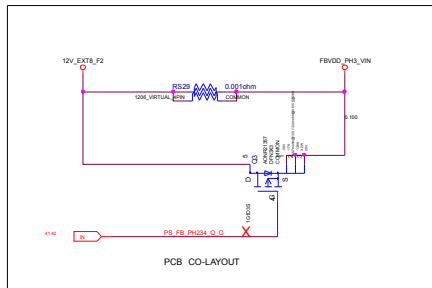
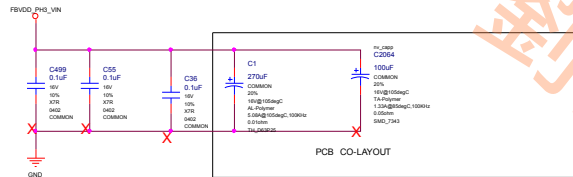
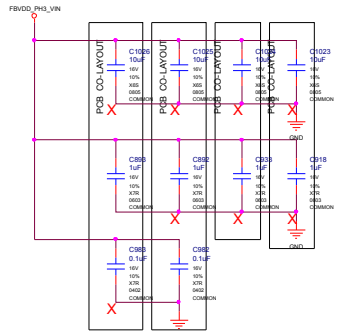
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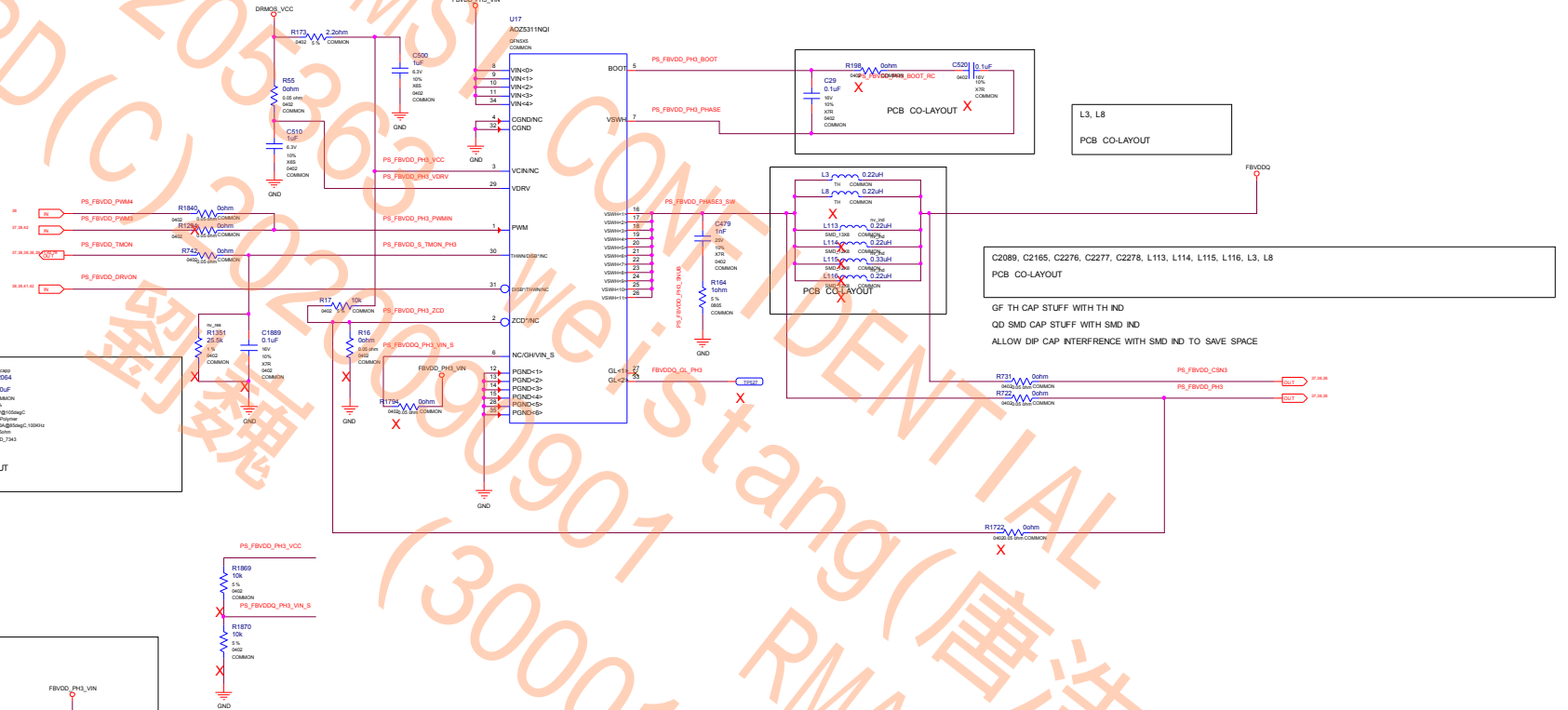
PS: FBVDD PH1



PS: FBVDD PH3

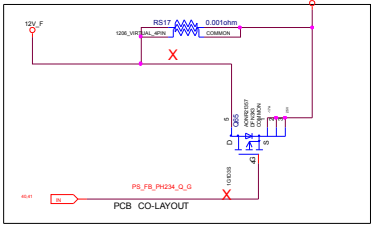
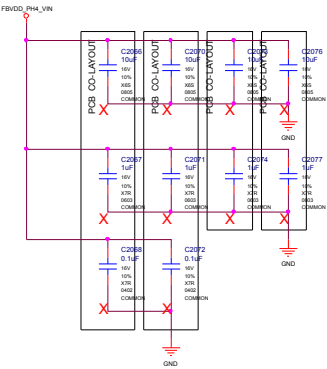


FBVDD PH3 INPUT ANTI-BACKDRIVE

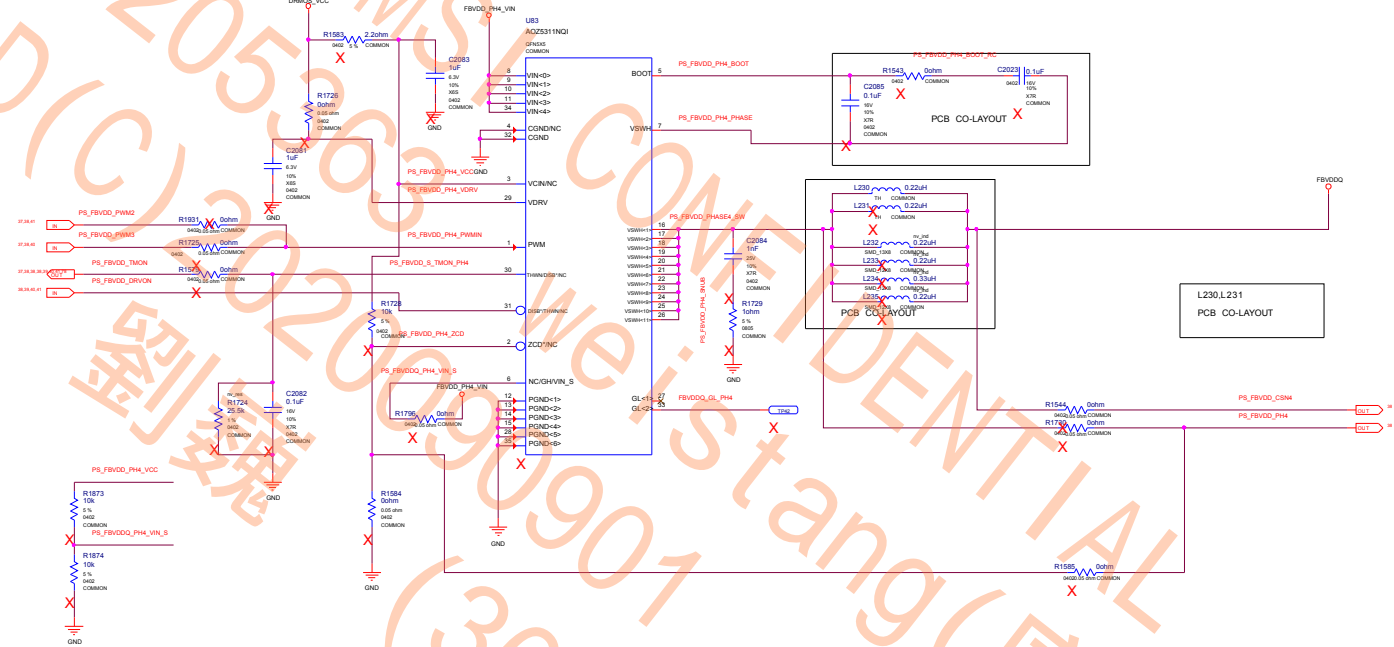
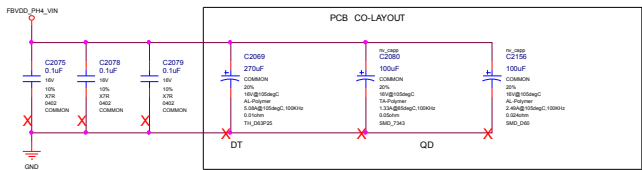


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PS: FBVDD PH4

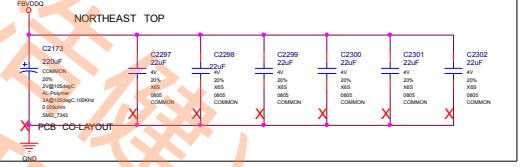
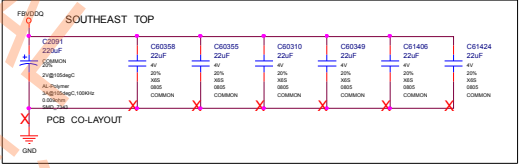
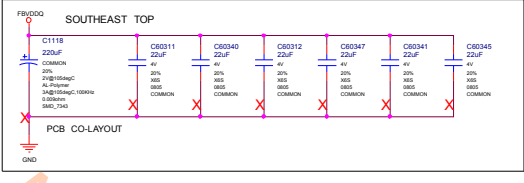
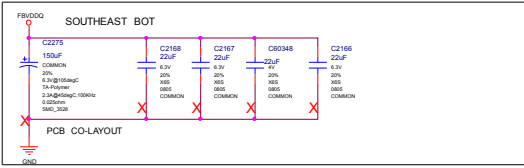
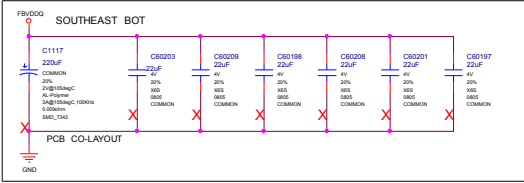
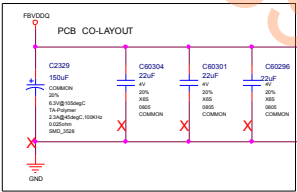
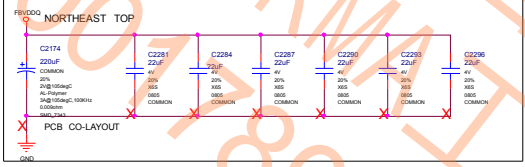
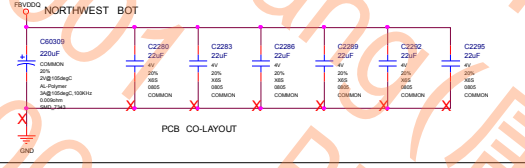
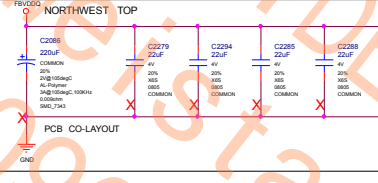
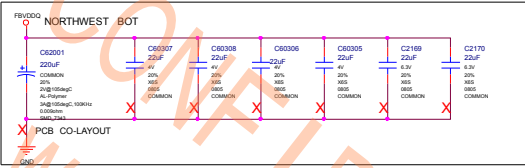
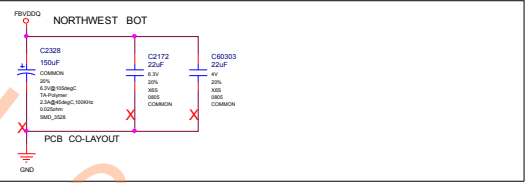
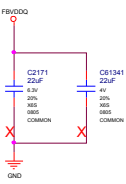
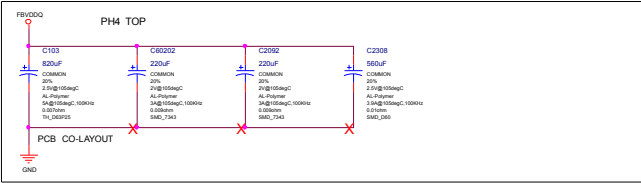
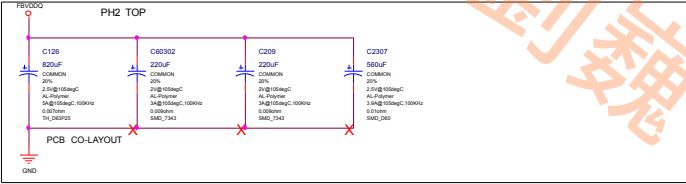
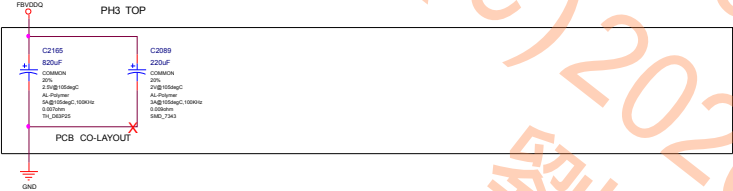


FBVDD PH3 INPUT ANTI-BACKDRIVE



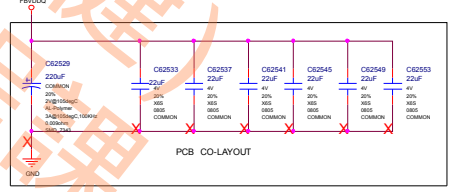
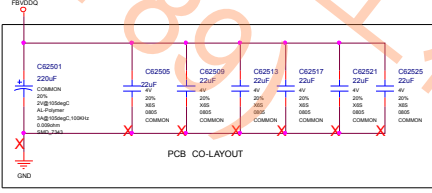
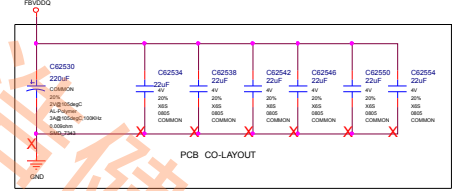
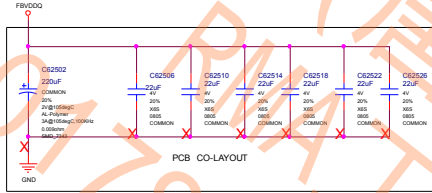
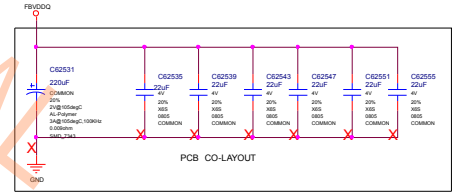
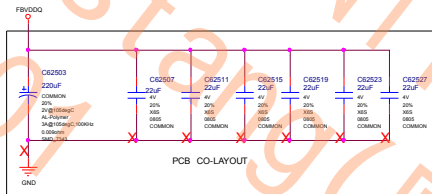
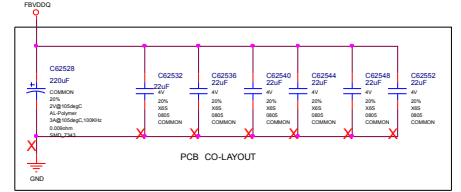
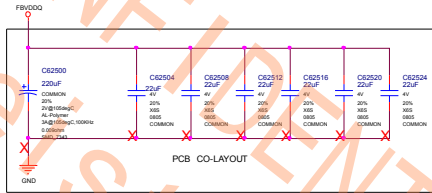
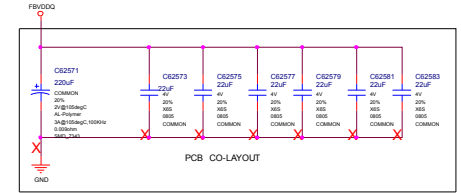
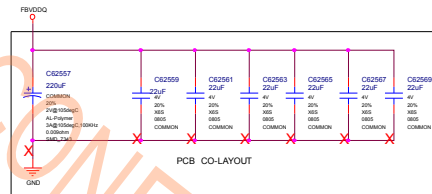
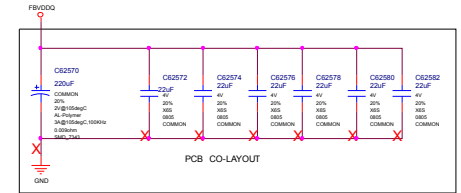
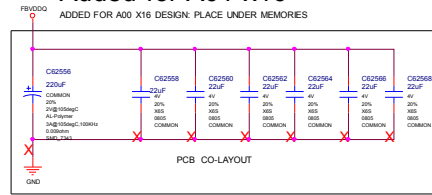
PS: FBVDD OUTPUT CAP

3x 820uF TH FBVDD OUTPUT BULK CAPS

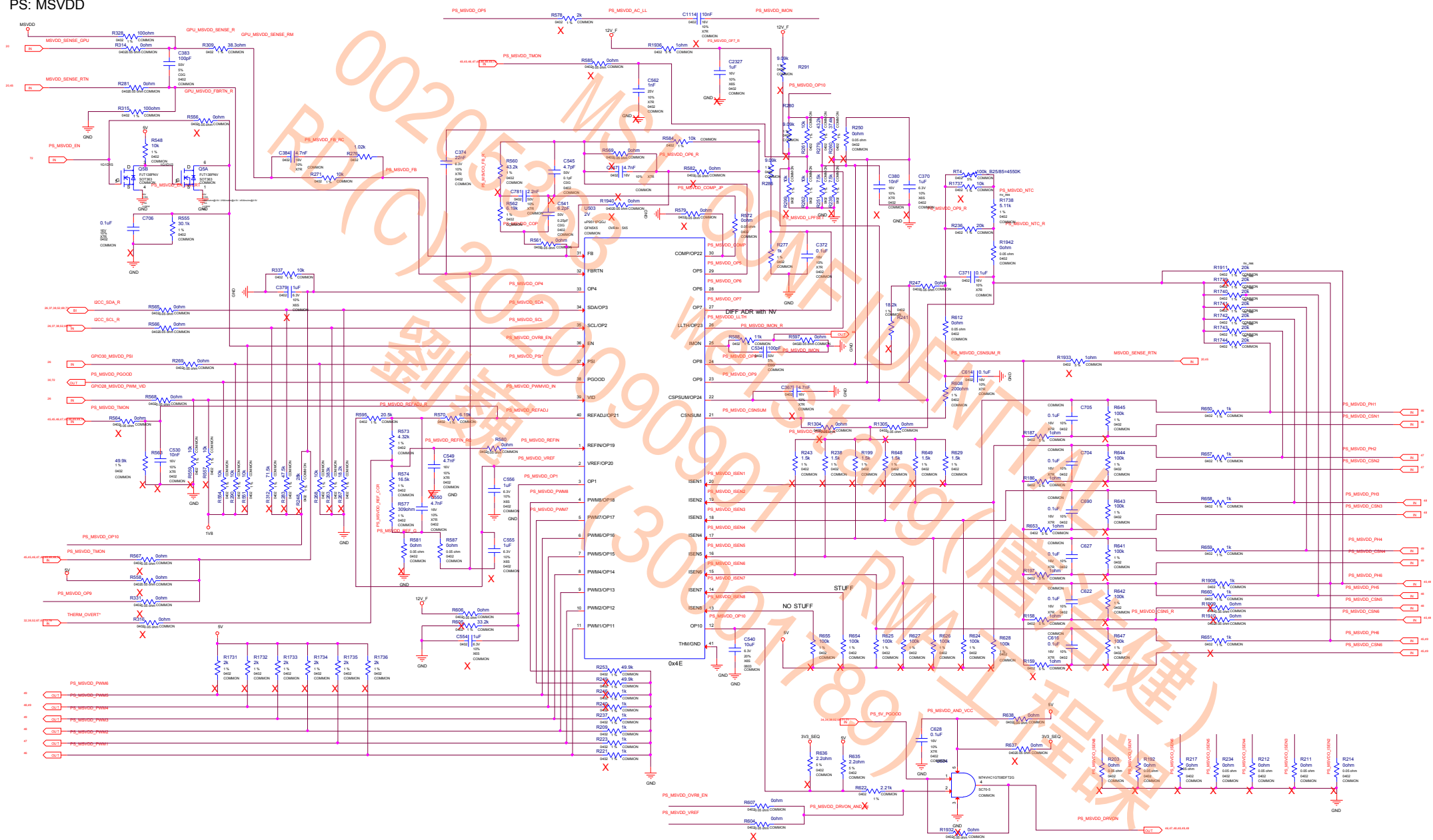


Added for A01 x16

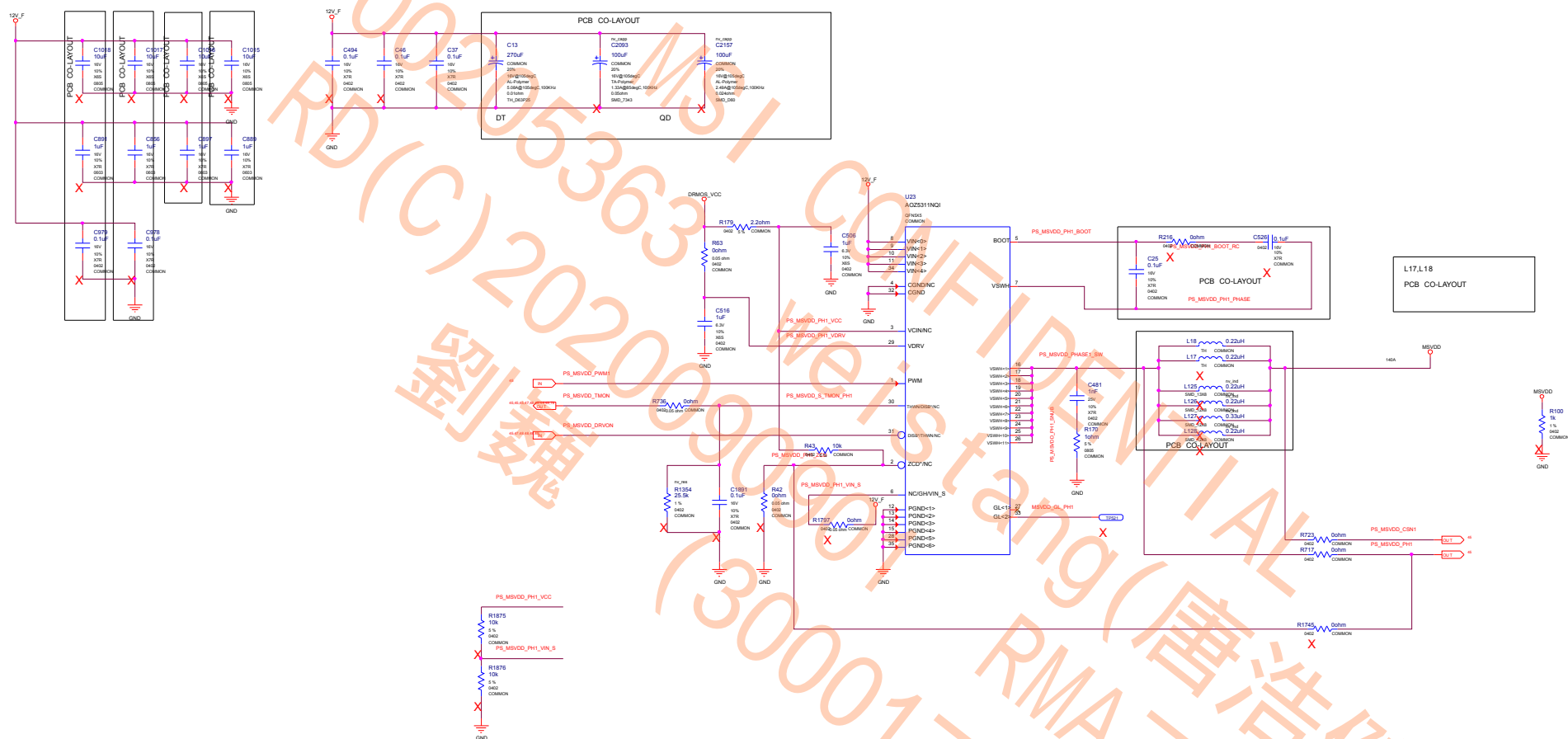
ADDED FOR A00 X16 DESIGN: PLACE UNDER MEMORIES

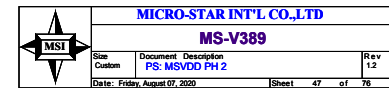
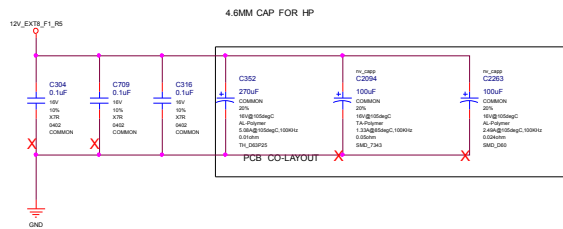


PS: MSVDD

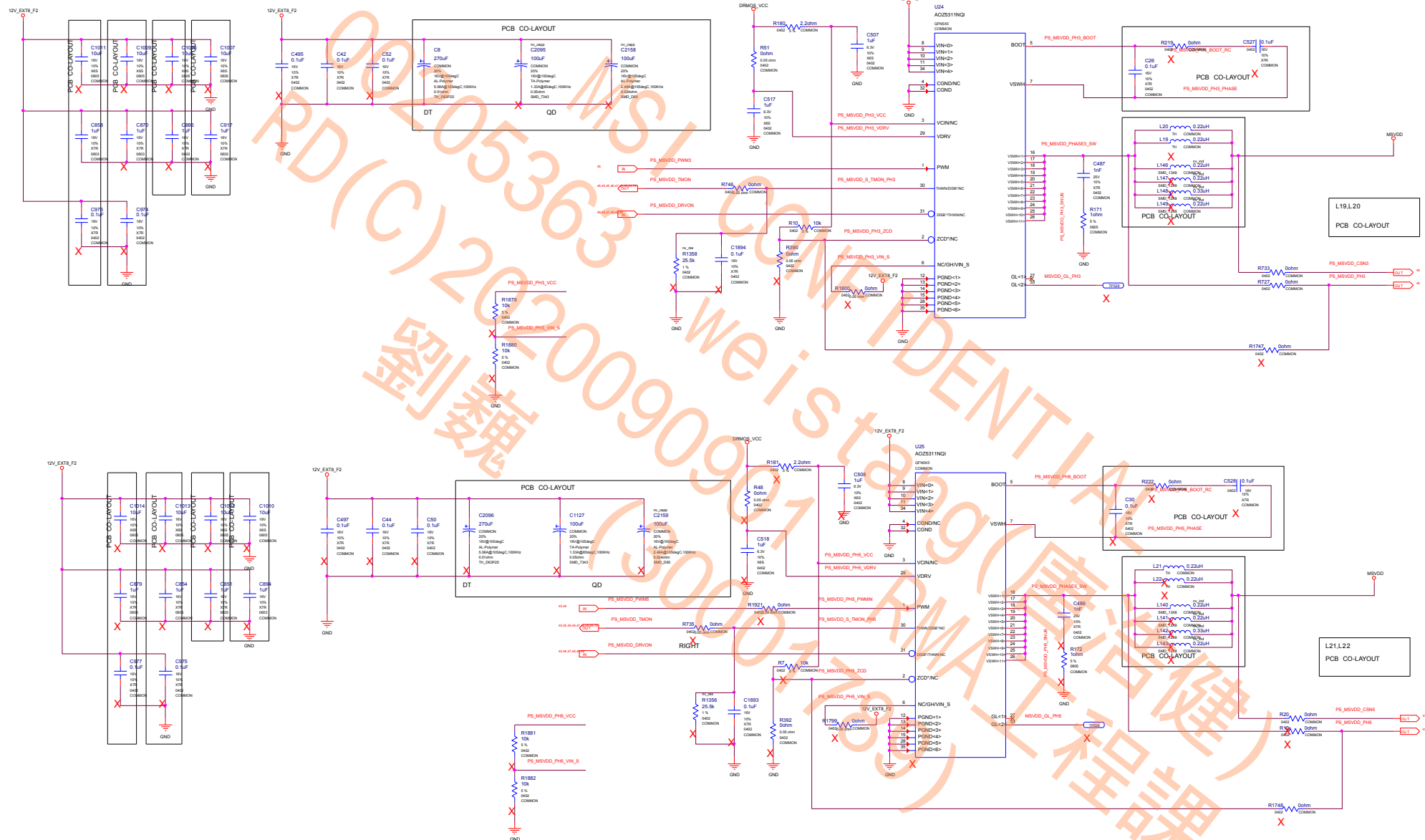


PS: MSVDD Phase 1

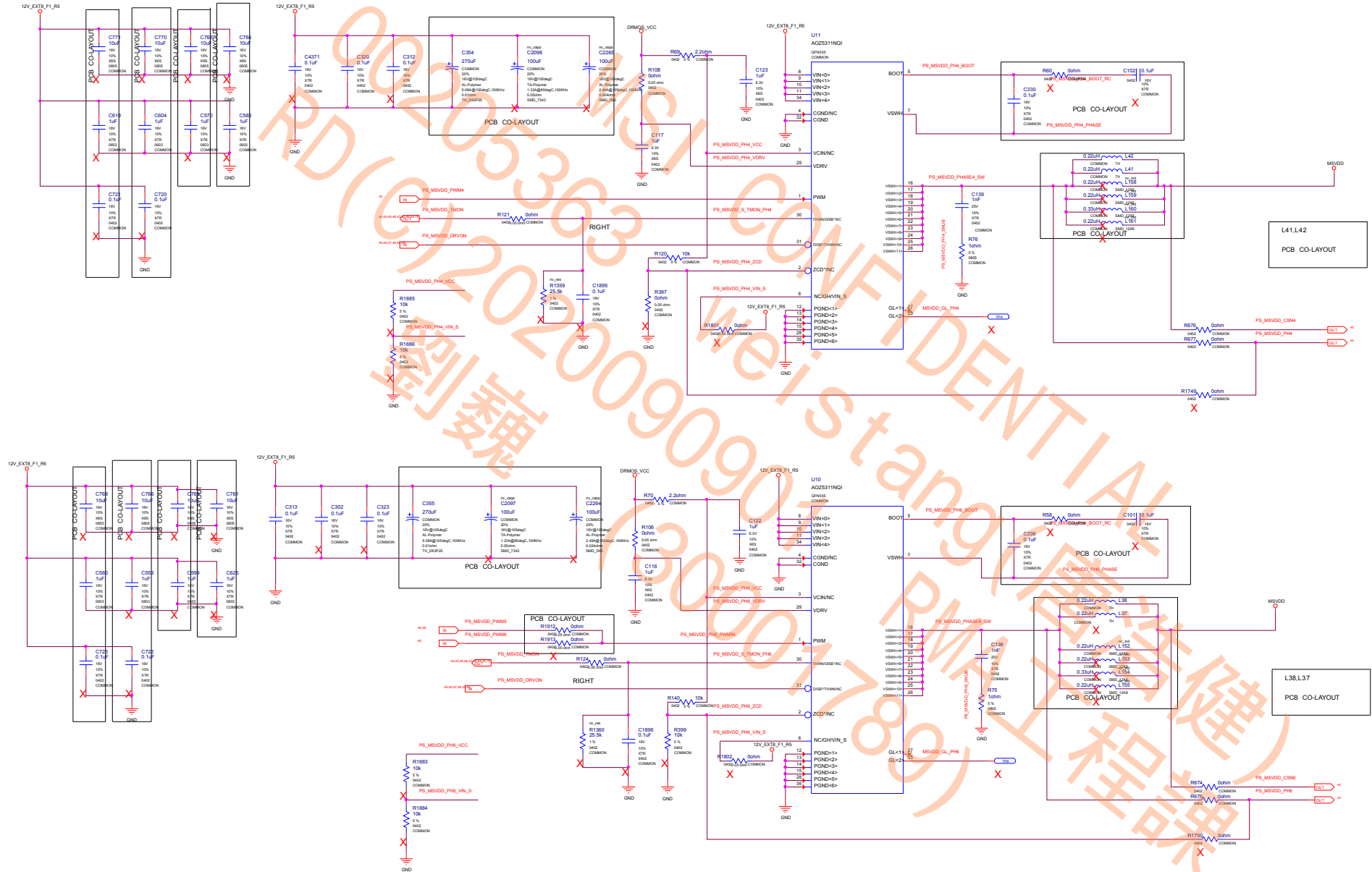




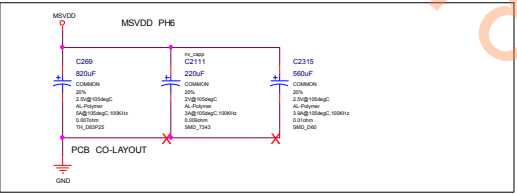
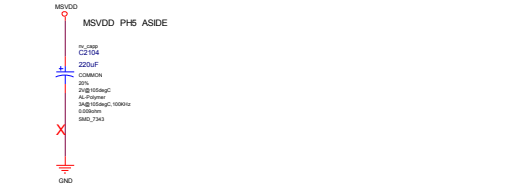
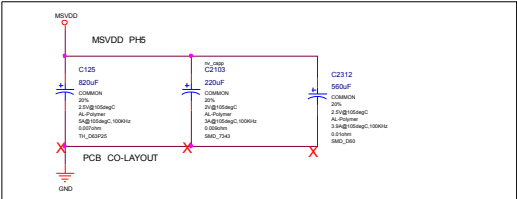
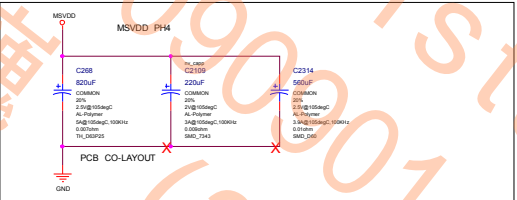
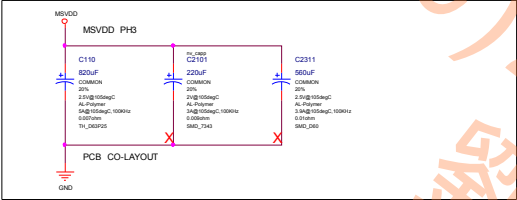
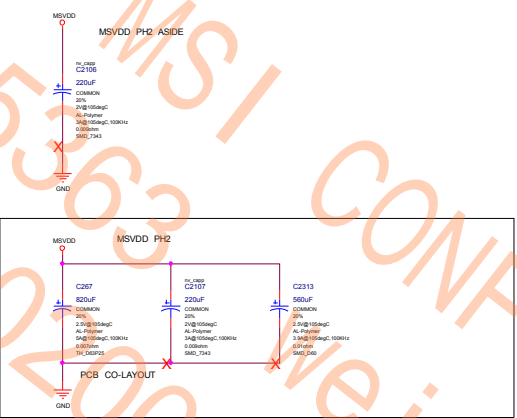
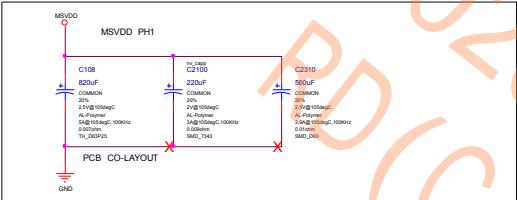
PS:MSVDD Phase 3, 5



PS: MSVDD PH 4,6



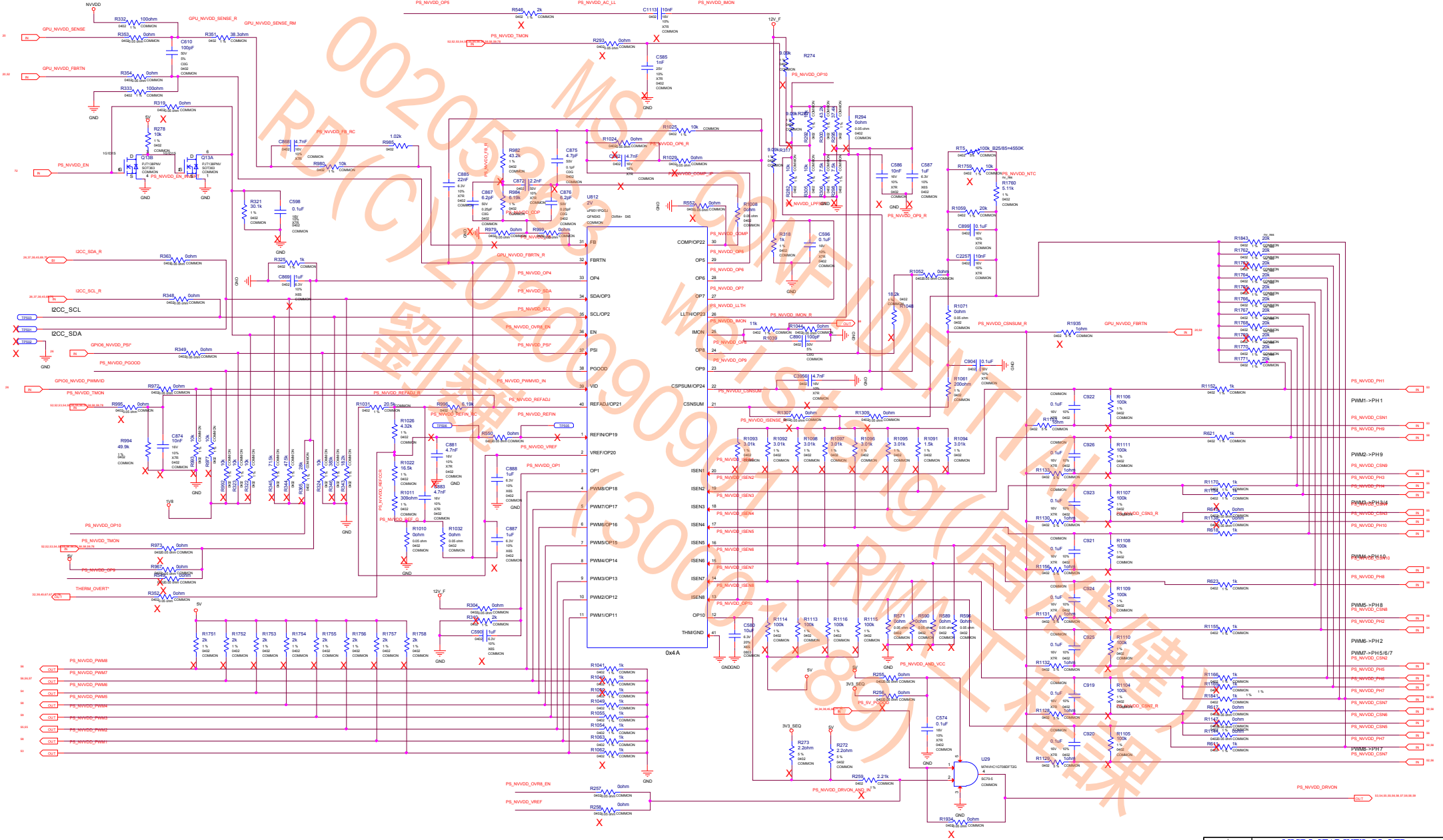
PS:MSVDD OUTPUT CAP (TOP)



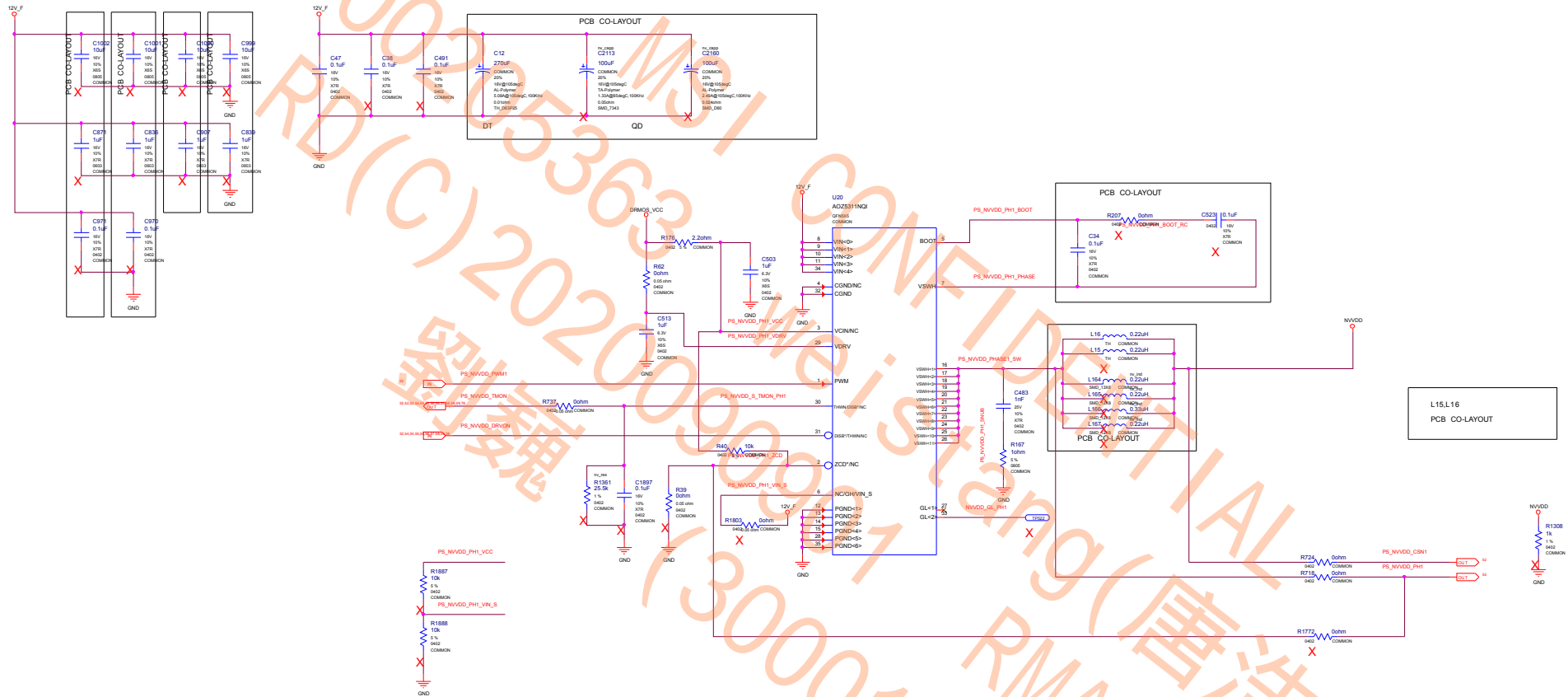
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MSI CONFIDENTIAL
weistang (唐浩健)
RMA工程課
(30001789)

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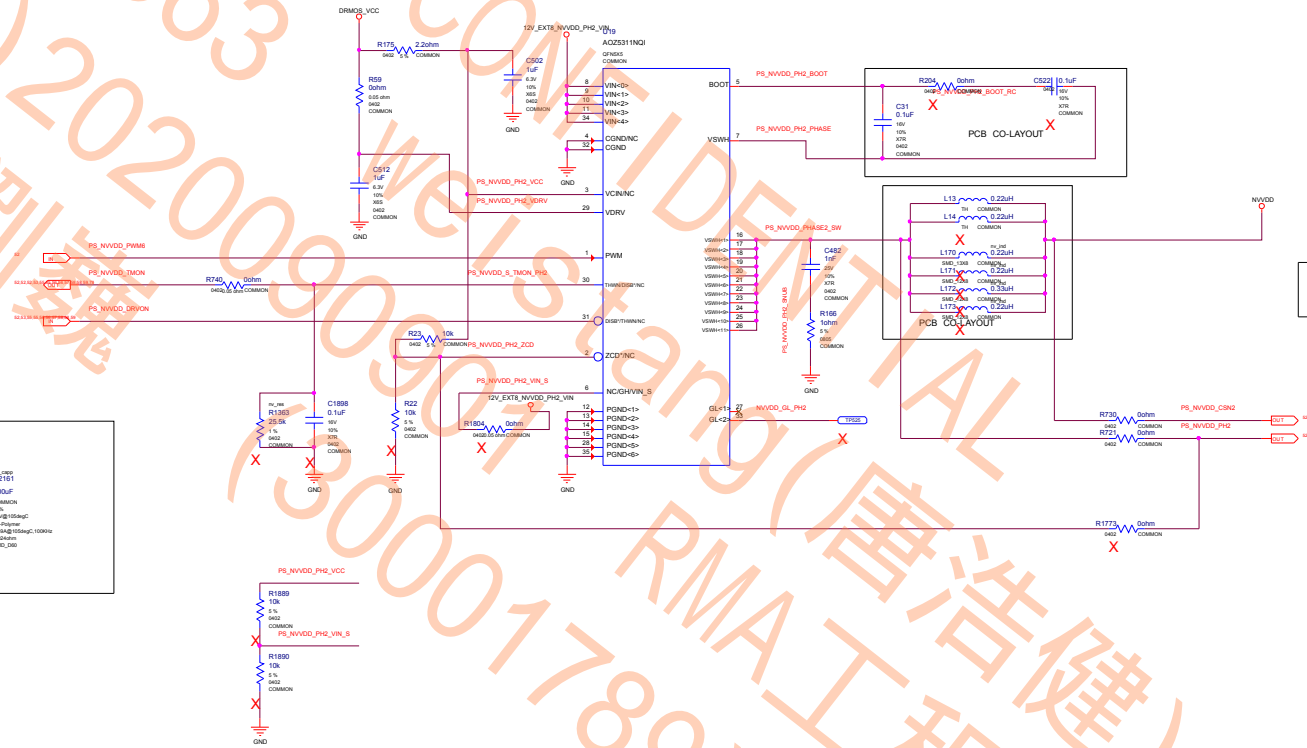
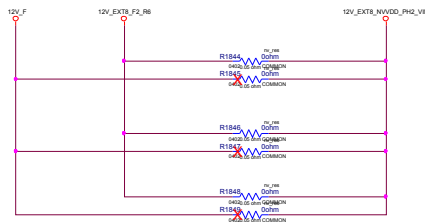
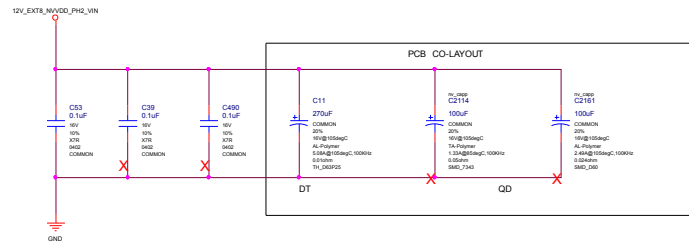
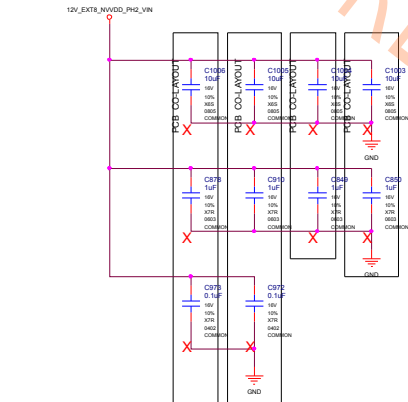
PS: NVVDD Controller_OVR8



PS: NVVDD Phase 1

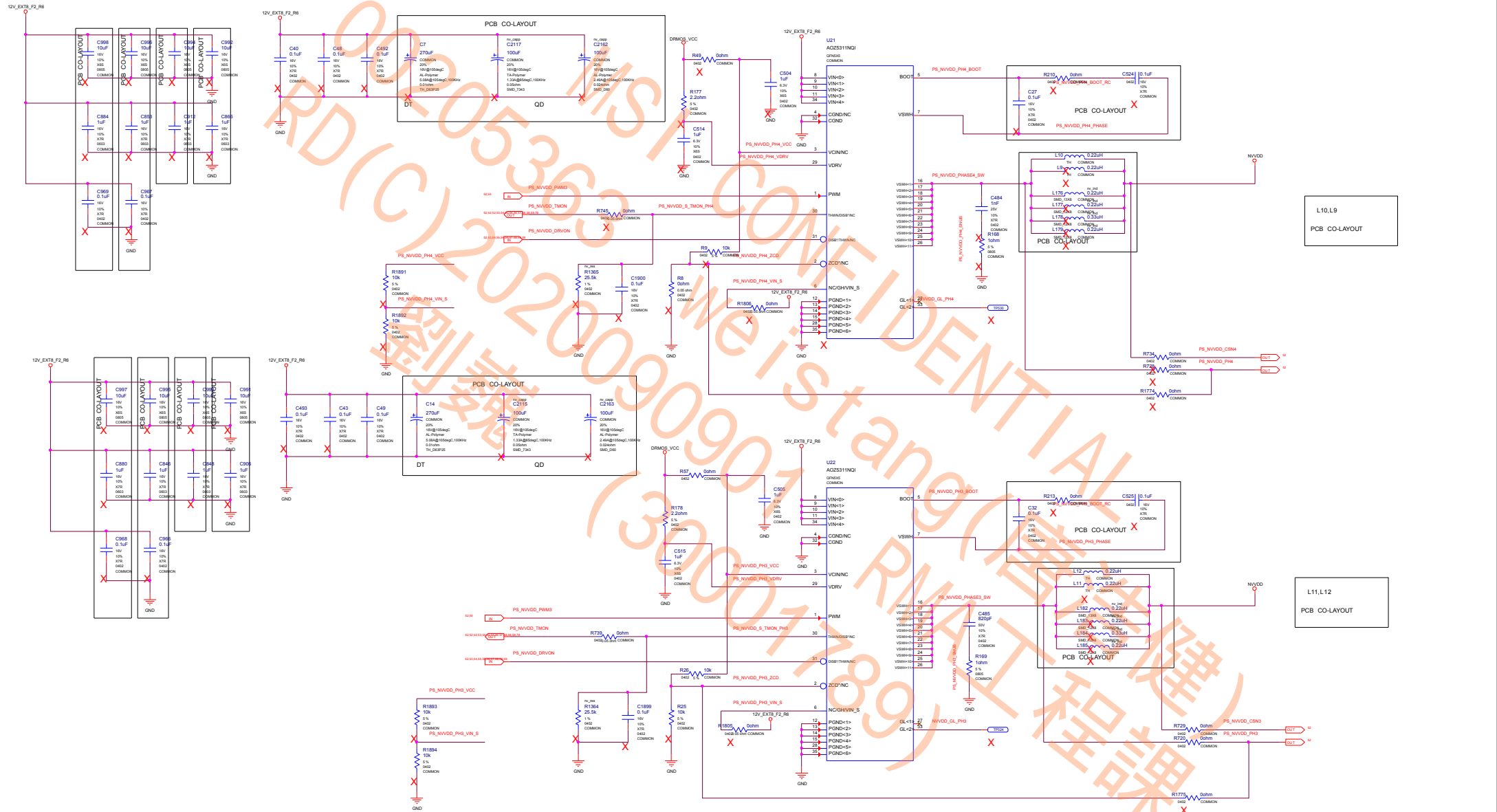


PS: NVVDD Phase 2

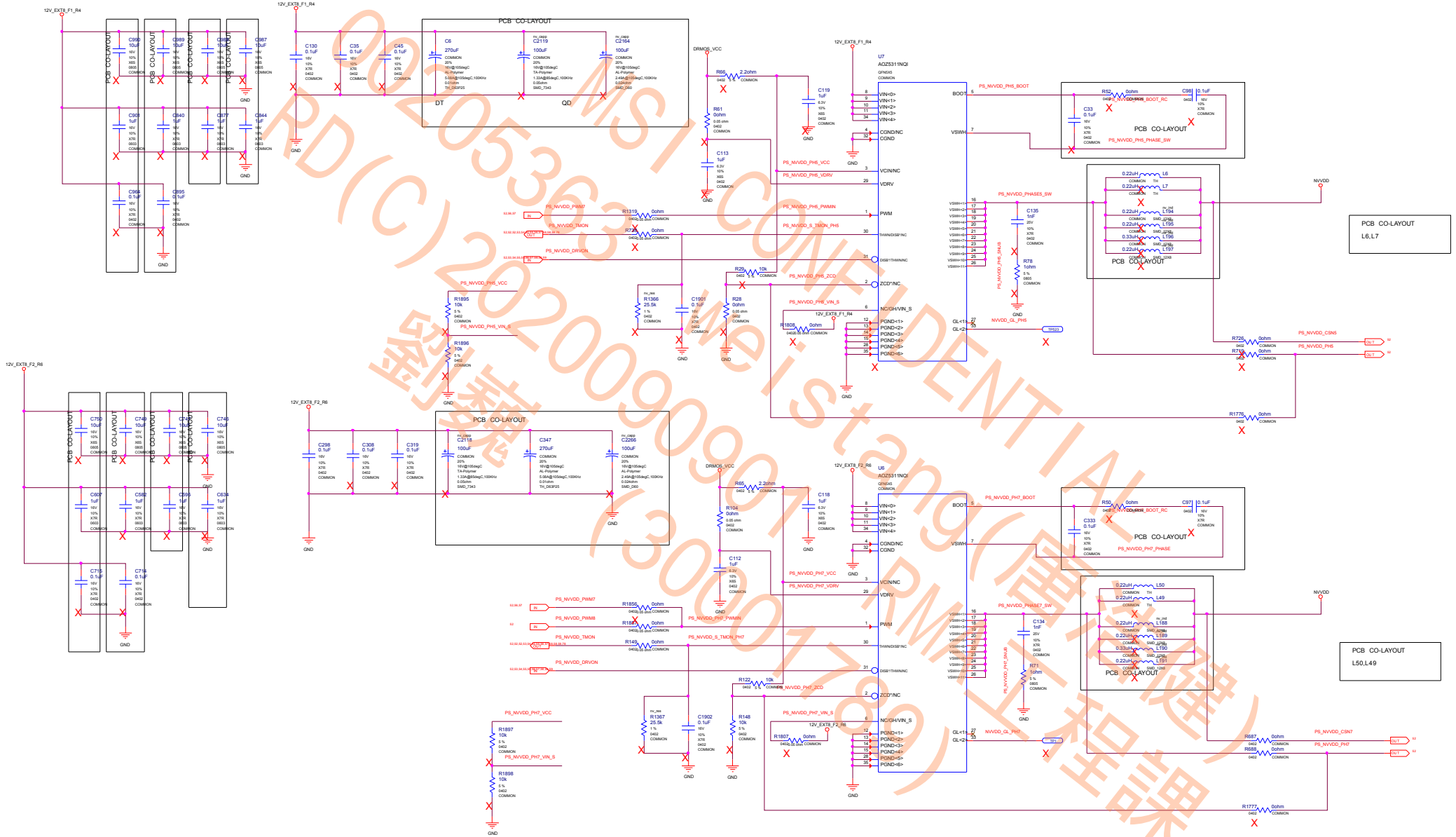


L13,L14
PCB CO-LAYOUT

PS: NVDD Phase 3 (PWM6), PHASE 4(PWM2)

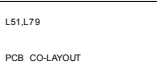
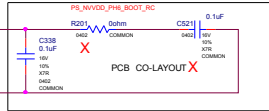
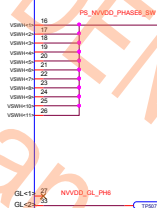
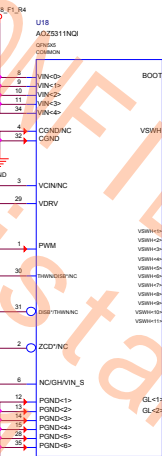
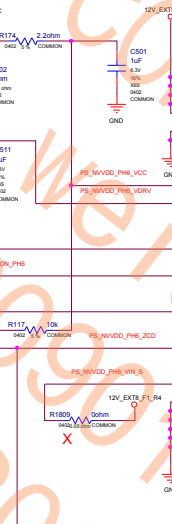
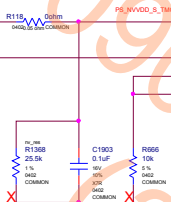
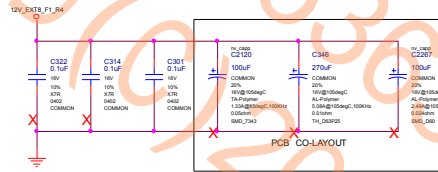
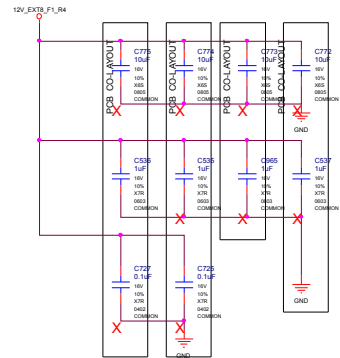


PS: NVVDD PH 5(PWM2), PH7(PWM3)

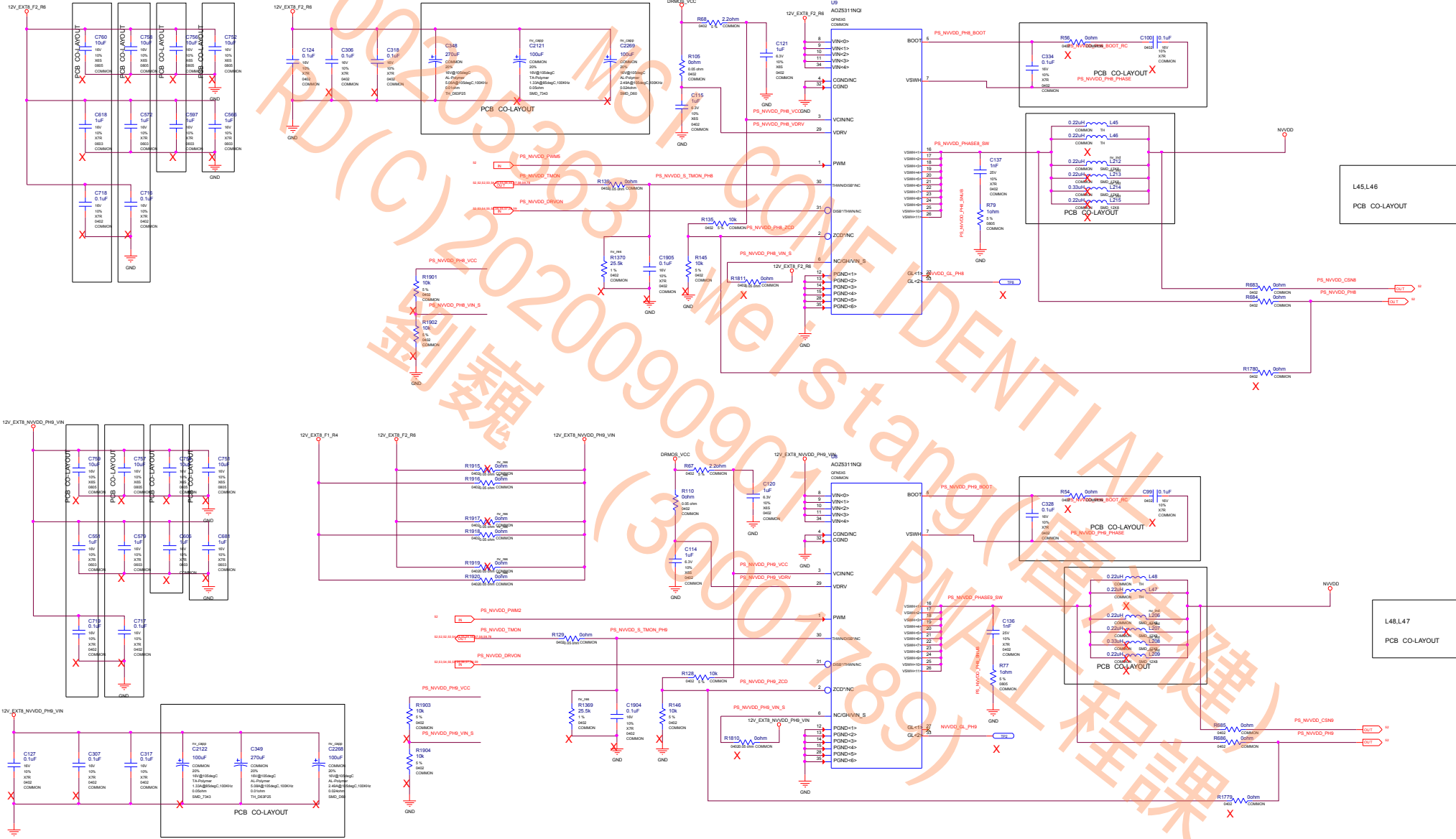


The diagram illustrates the PCB layout for the PS_NVDD_PHS_VCC section. It includes several key components and connections:

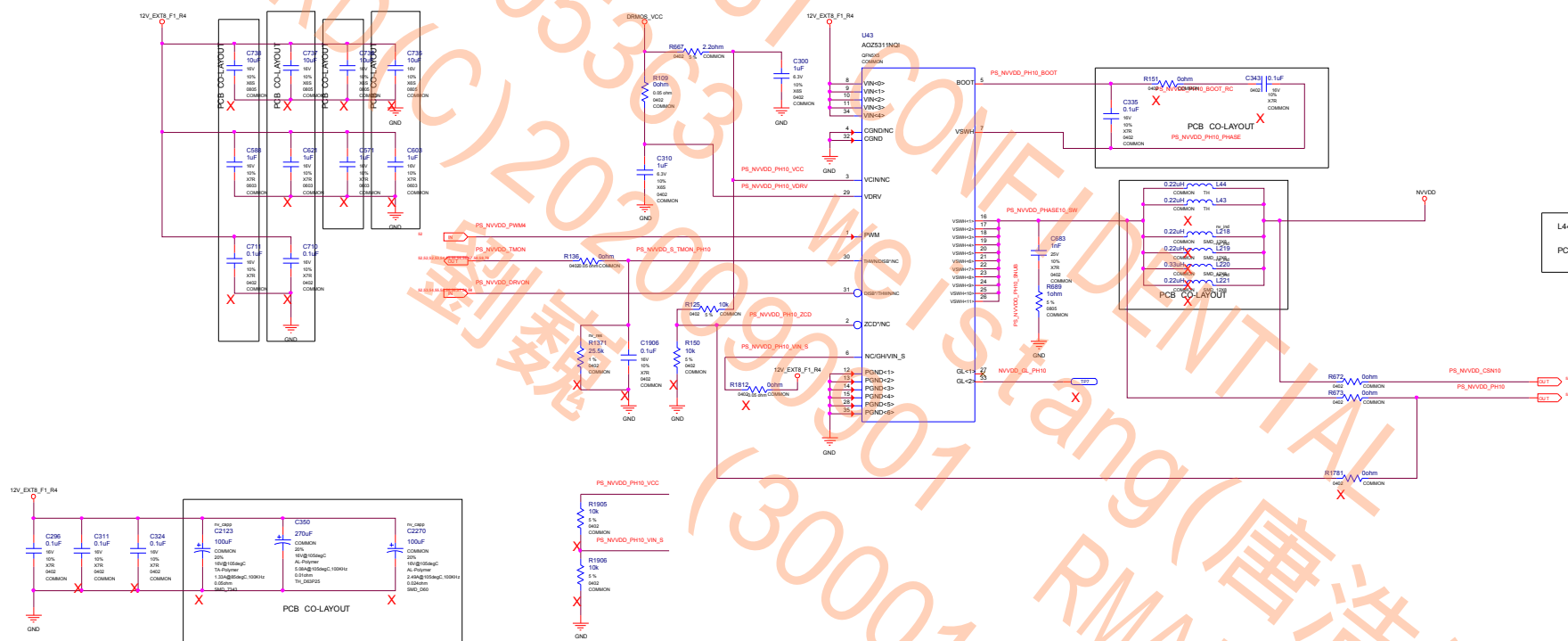
- Capacitors:** C322 (0.1uF), C314 (0.1uF), C301 (0.1uF), C210 (100uF), C340 (270uF), C205 (10uF), C300 (10uF), C302 (10uF), C303 (10uF), C304 (10uF), C305 (10uF), C306 (10uF), C307 (10uF), C308 (10uF), C309 (10uF), C310 (10uF), C311 (10uF), C312 (10uF), C313 (10uF), C314 (10uF), C315 (10uF), C316 (10uF), C317 (10uF), C318 (10uF), C319 (10uF), C320 (10uF), C321 (10uF), C322 (10uF), C323 (10uF), C324 (10uF), C325 (10uF), C326 (10uF), C327 (10uF), C328 (10uF), C329 (10uF), C330 (10uF), C331 (10uF), C332 (10uF), C333 (10uF), C334 (10uF), C335 (10uF), C336 (10uF), C337 (10uF), C338 (10uF), C339 (10uF), C340 (10uF), C341 (10uF), C342 (10uF), C343 (10uF), C344 (10uF), C345 (10uF), C346 (10uF), C347 (10uF), C348 (10uF), C349 (10uF), C350 (10uF), C351 (10uF), C352 (10uF), C353 (10uF), C354 (10uF), C355 (10uF), C356 (10uF), C357 (10uF), C358 (10uF), C359 (10uF), C360 (10uF), C361 (10uF), C362 (10uF), C363 (10uF), C364 (10uF), C365 (10uF), C366 (10uF), C367 (10uF), C368 (10uF), C369 (10uF), C370 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PS: NVVDD PH 8 (PWM5), PH 9(PWM8)



PS: NVVDD Phase 10 (PWM8)



PCB CO-LAYOUT

C131, C132, C133, C140, C141, C142, C2106, C2107, C2133, C2134, C2135, C2137, C264, C265, C266, C267, C61, C64, C65, C66, C67, C68, C69, C77, C80, C83, C88

PCB CO-LAYOUT

C103, C105, C106, C107, C108, C110, C1208, C125, C1254, C1256, C1267, C128, C144, C145, C146, C151, C152, C153, C154, C159, C160, C161, C162, C170, C173, C2092, C2100, C2101, C2102, C2103, C2104, C2138, C2139, C2140, C2141, C2142, C2143, C2144, C2272, C230, C231, C232, C233, C243, C245, C246, C248, C253, C254, C255, C256, C270, C274, C275, C276, C283, C289, C290, C291, C60202, C62004, C62005

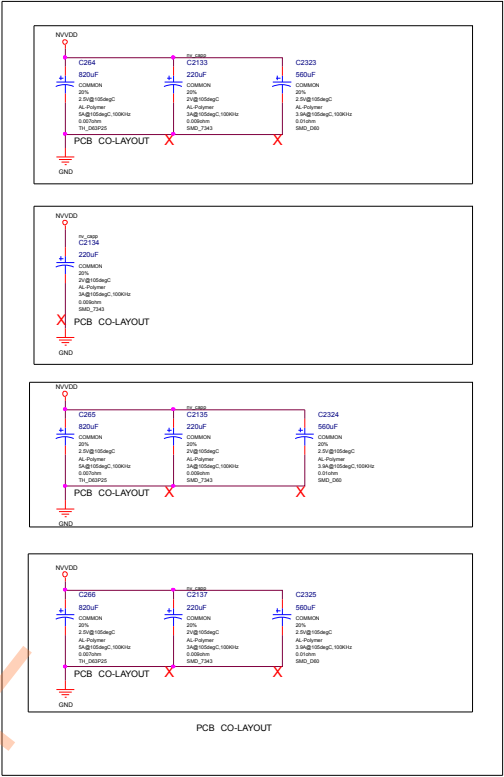
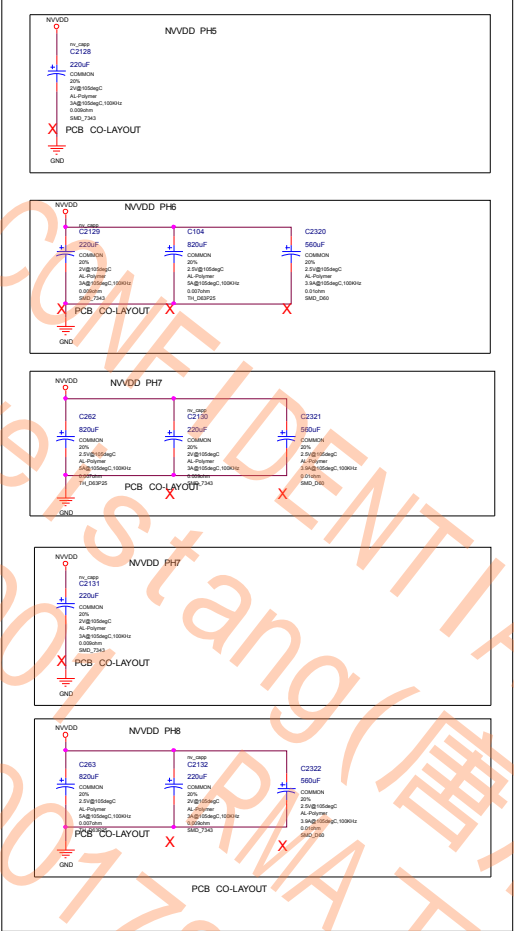
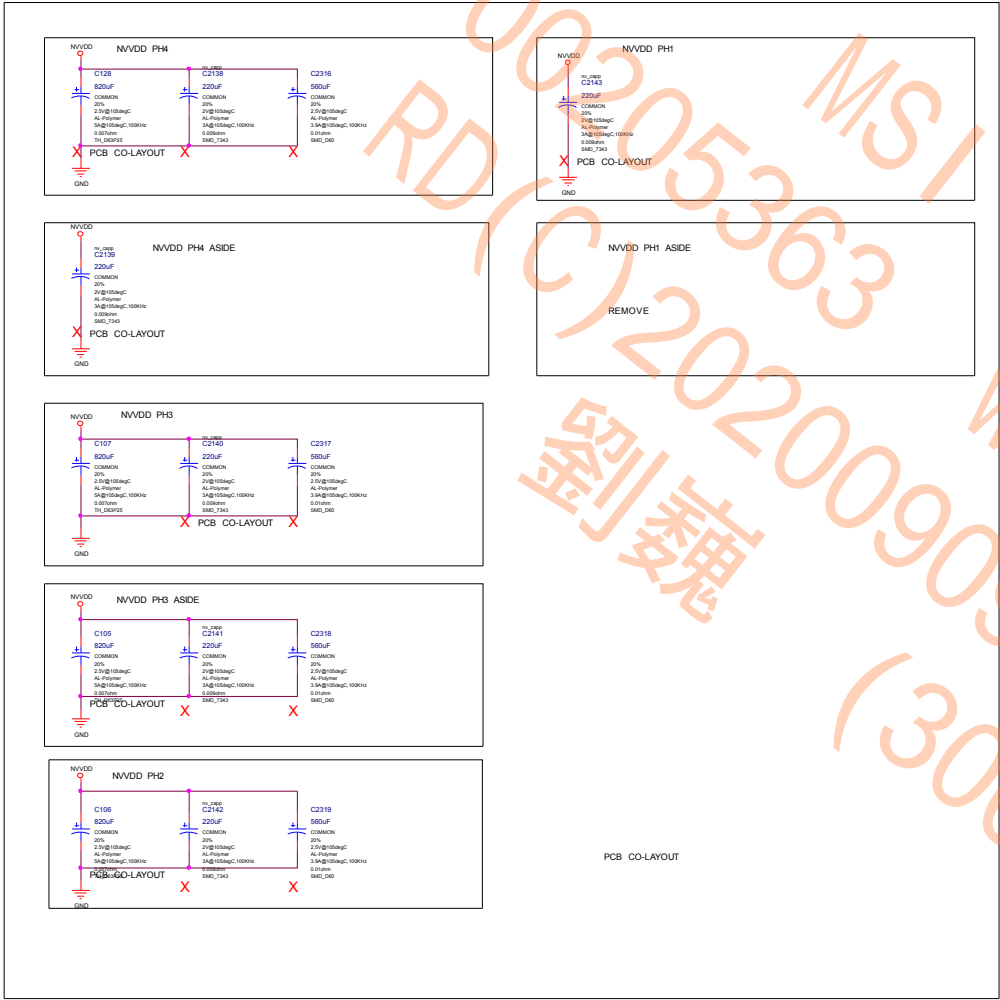
C163, C164, C166, C167, C2087, C2105, C2109, C2110, C2111, C224, C225, C261, C268, C269, C60354, C61428, C62, C63, C89, C91, C96

PCB CO-LAYOUT

2020_06_17
1.Fix J1,J2 to reverse 8 pins
2.Change L238,L52,L53 footprint

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劉魏
(30001789)
RMA工程課

PS: NVDD OUTPUT CAP(TOP)

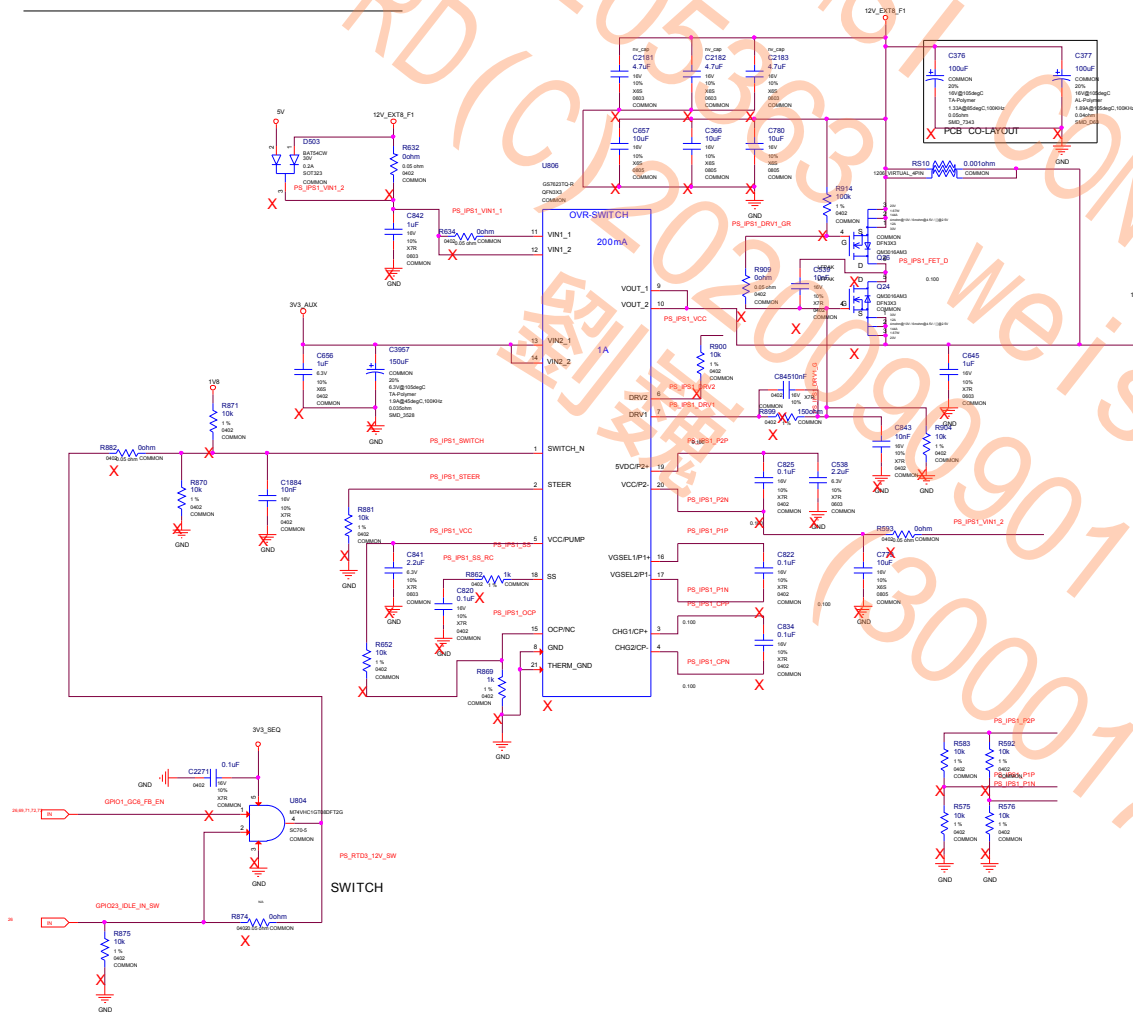


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RD(C)20200901
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(30001789) RMA工程課

PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

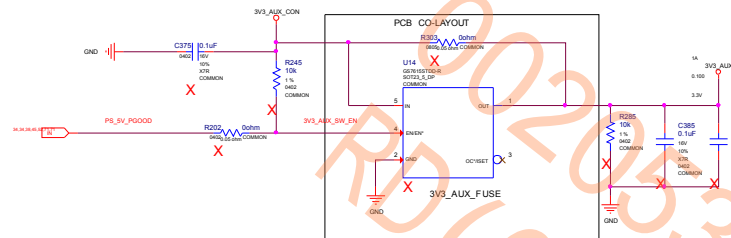
GPIO1	GPIO23	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A



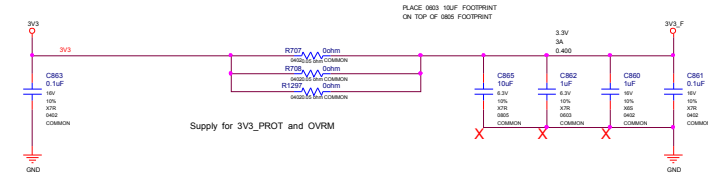
MSI CONFIDENTIAL
00205363
RD(C)2020090901
weistang (唐浩健)
RMA工程課
(30001789)

BLANK

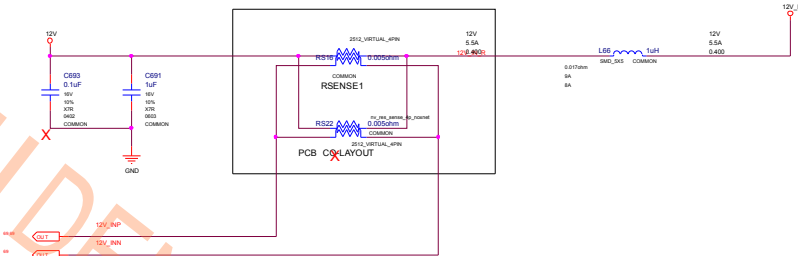
PS: Inputs, Filtering, and Monitoring



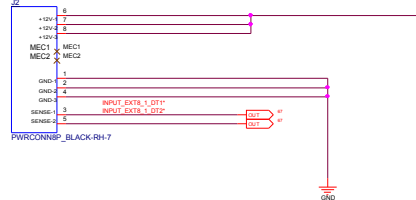
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W

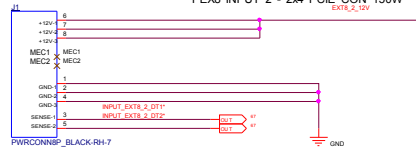


PEX8 INPUT 1 - 2x4 PCIe CON 150W

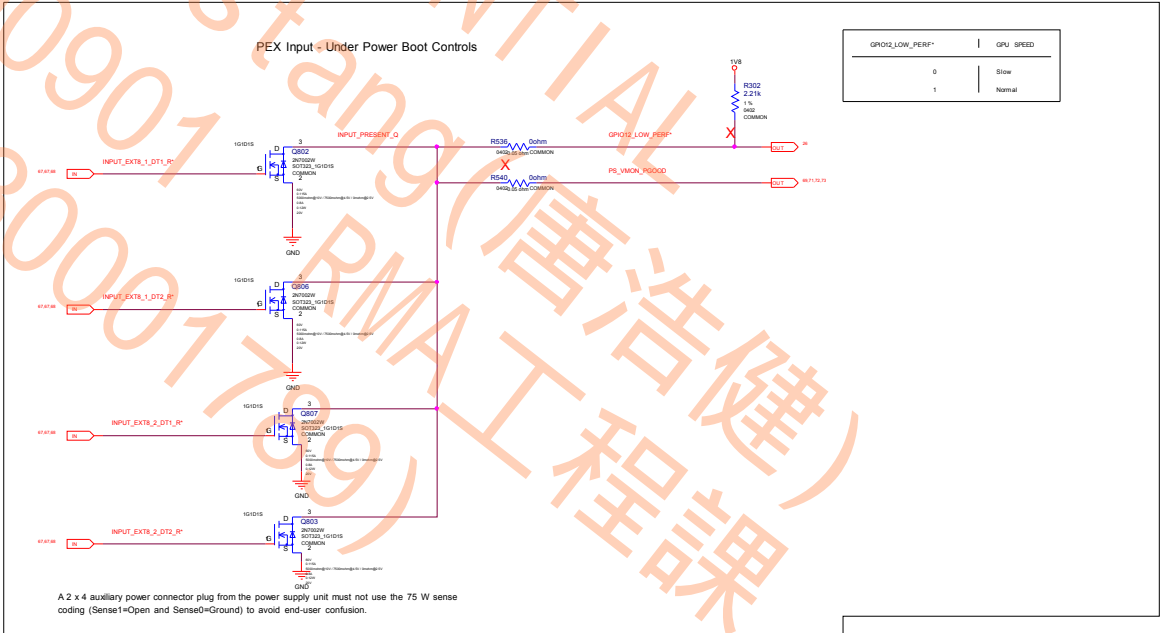
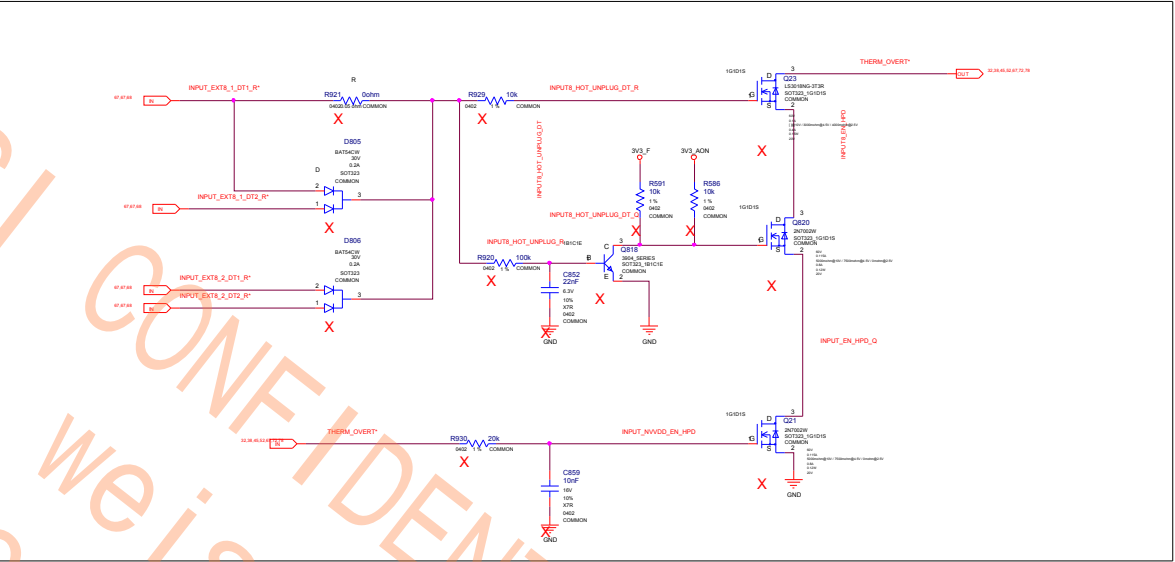
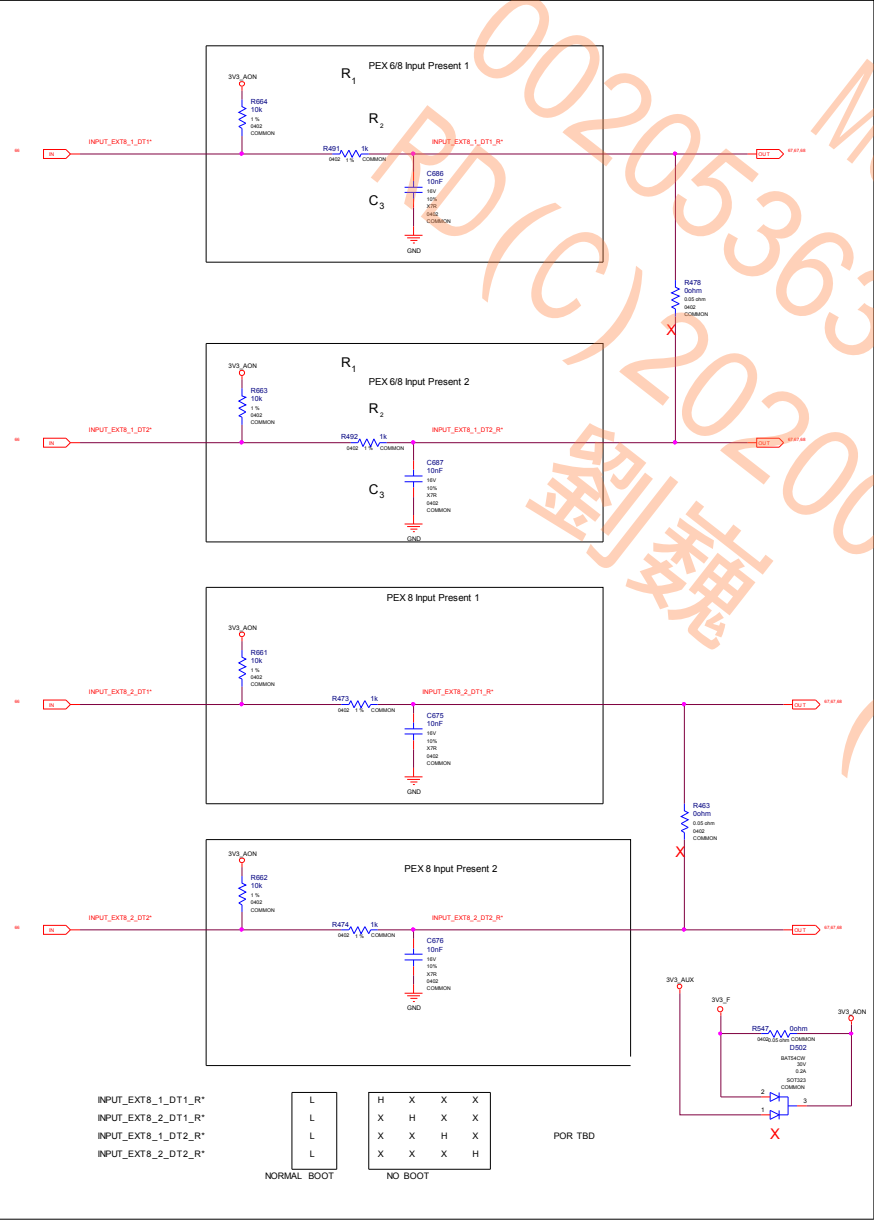


QD SKU CABLE

PEX8 INPUT 2 - 2x4 PCIe CON 150W



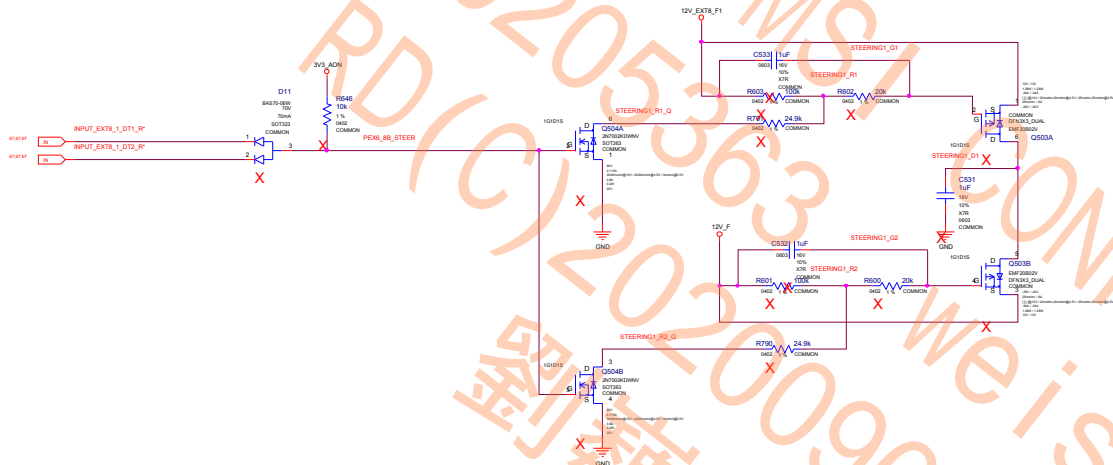
PS: 12V Current Steering & Hot Unplug Detect



PS: Discrete Steering

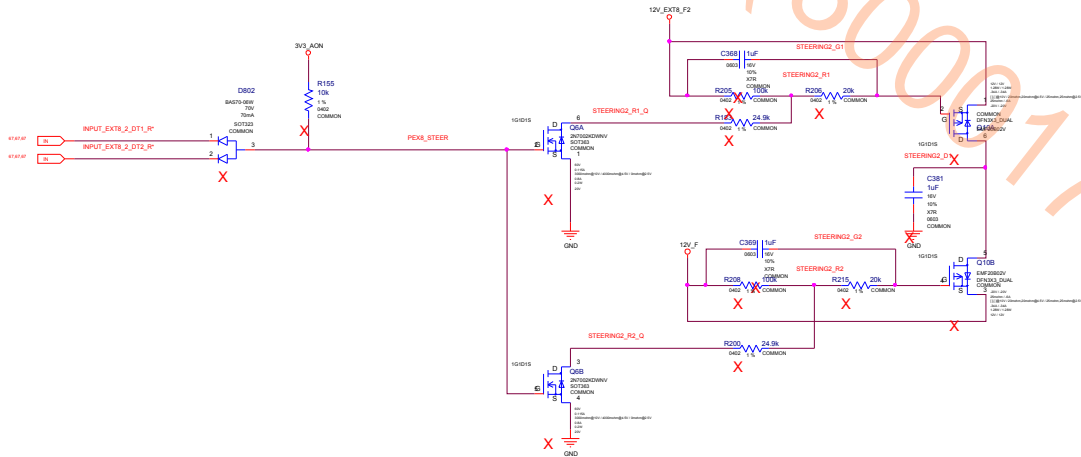
12V CURRENT STEERING (UNDER POWER BOOT):

PEX12V AND 12V_EXT8_F1



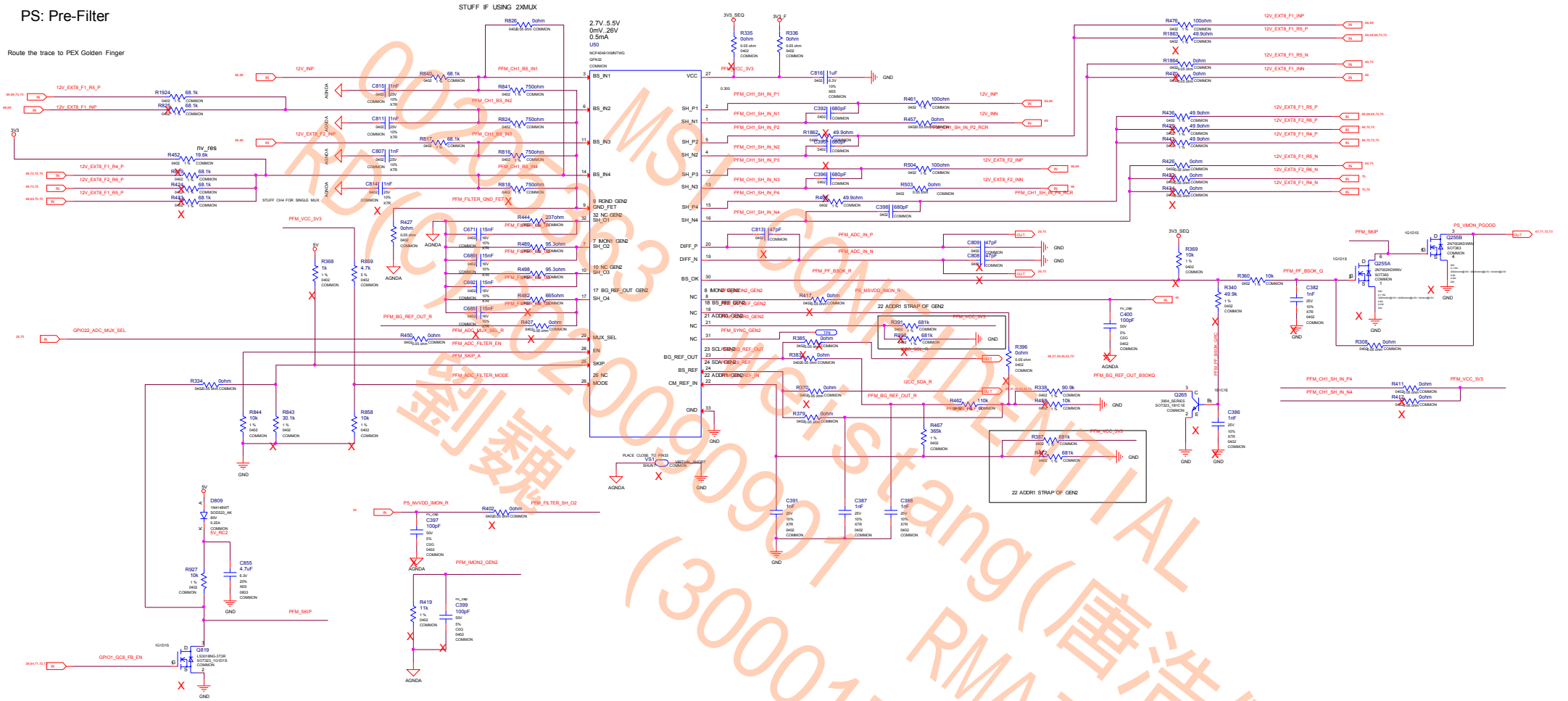
NO STUFF BY DEFAULT REF ONLY

PEX12V AND 12V_EXT8_F2

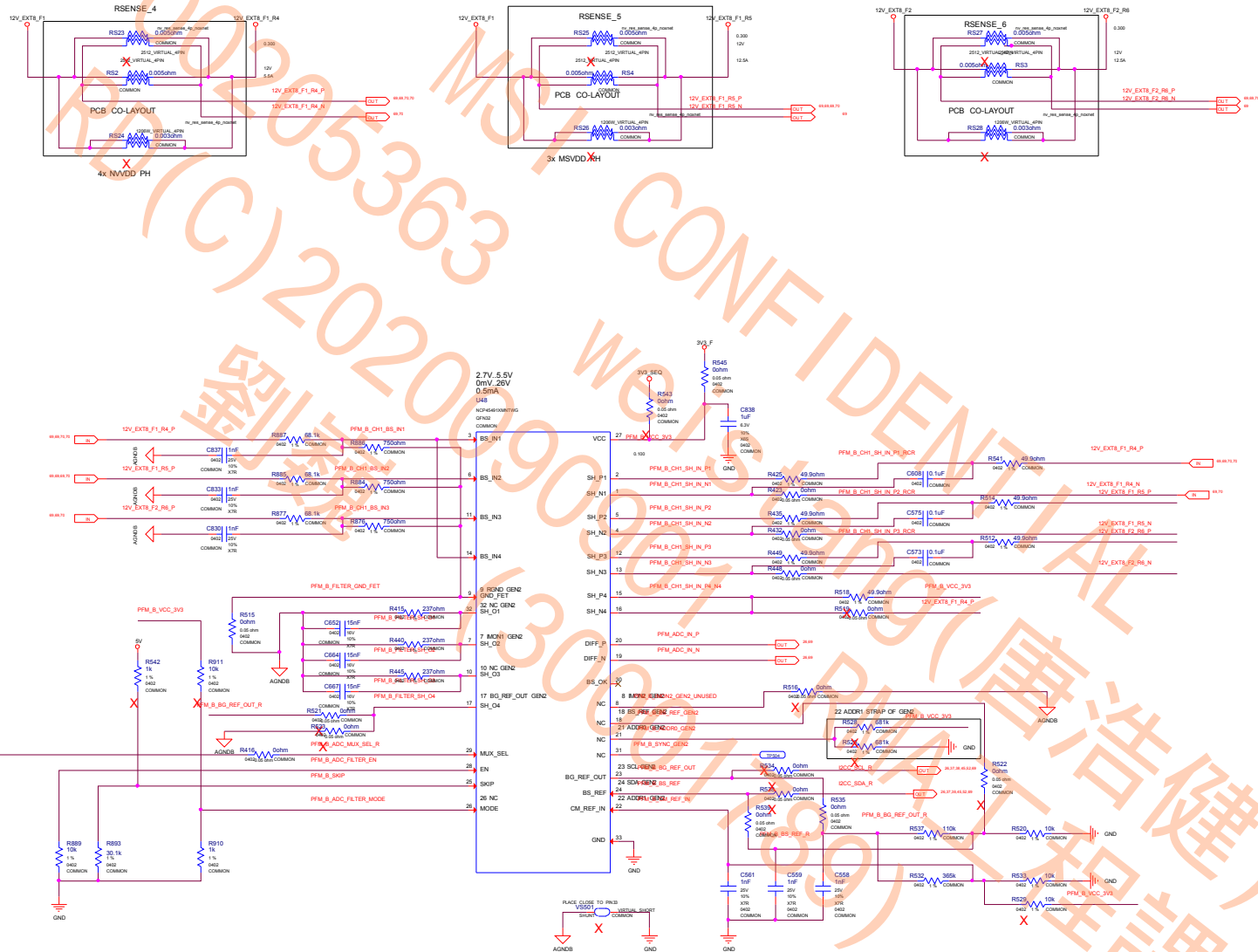


PS: Pre-Filter

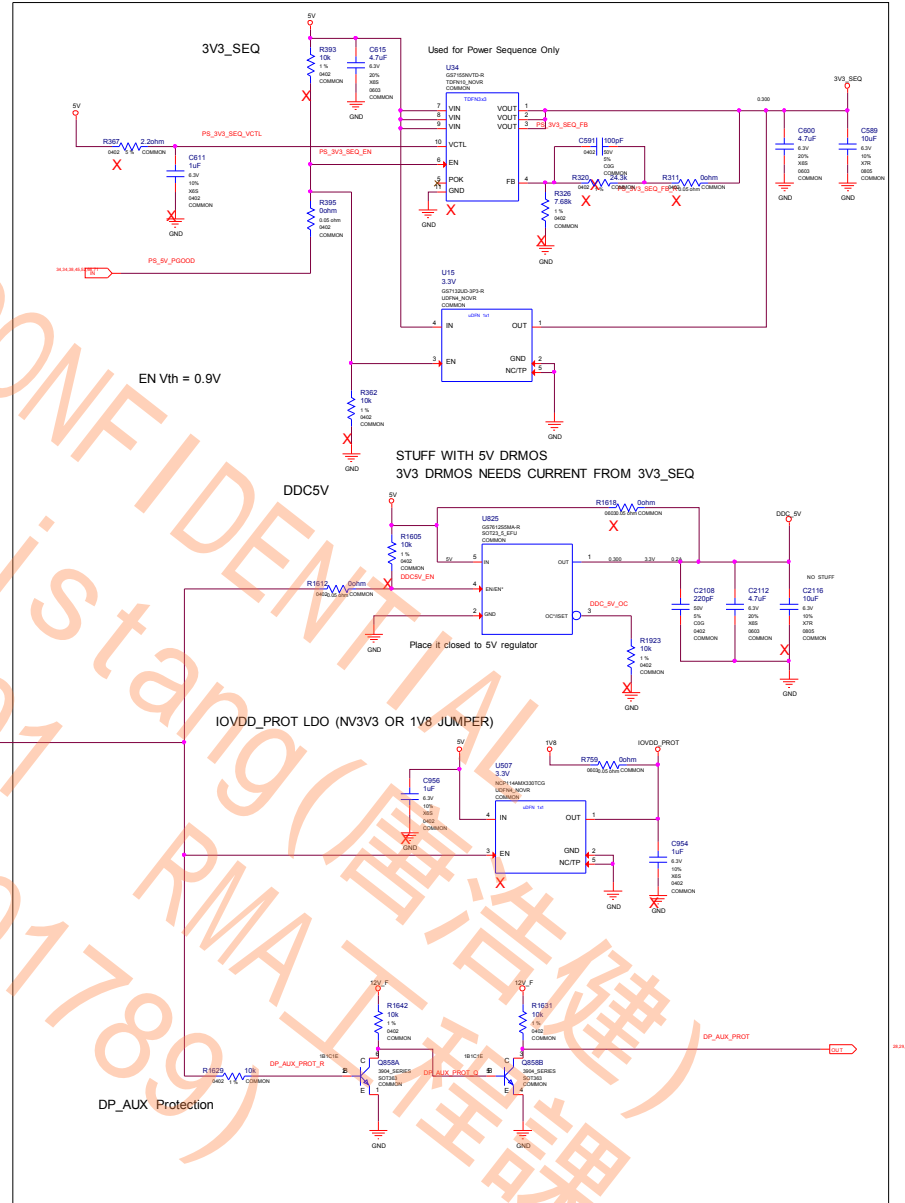
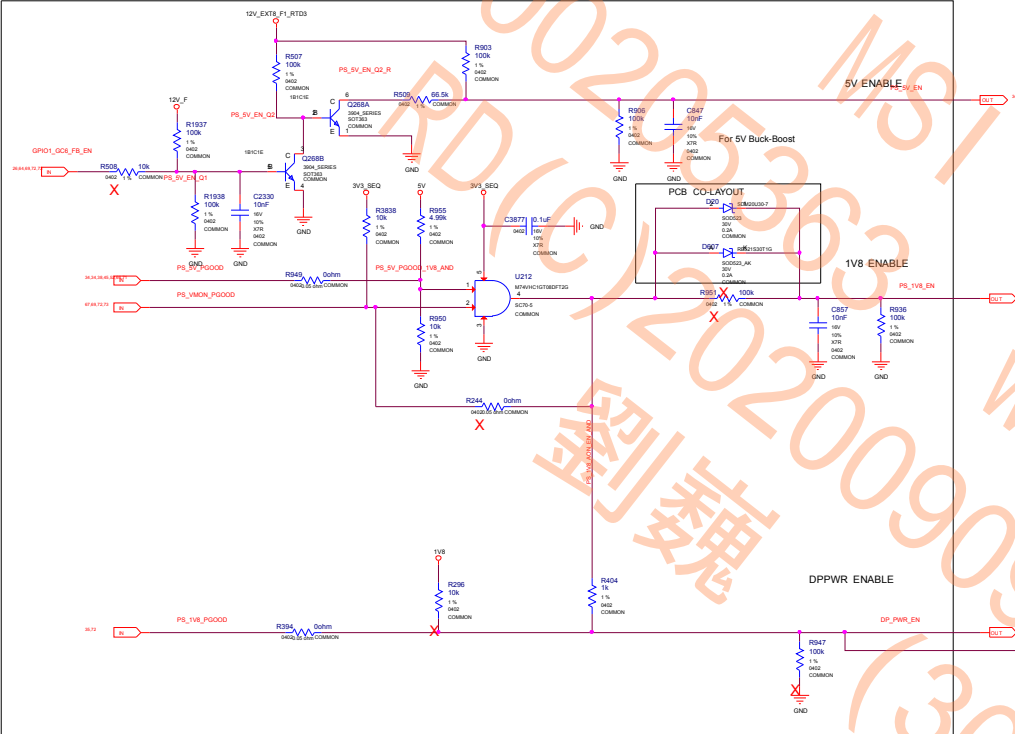
Route the trace to PEX Golden Finger



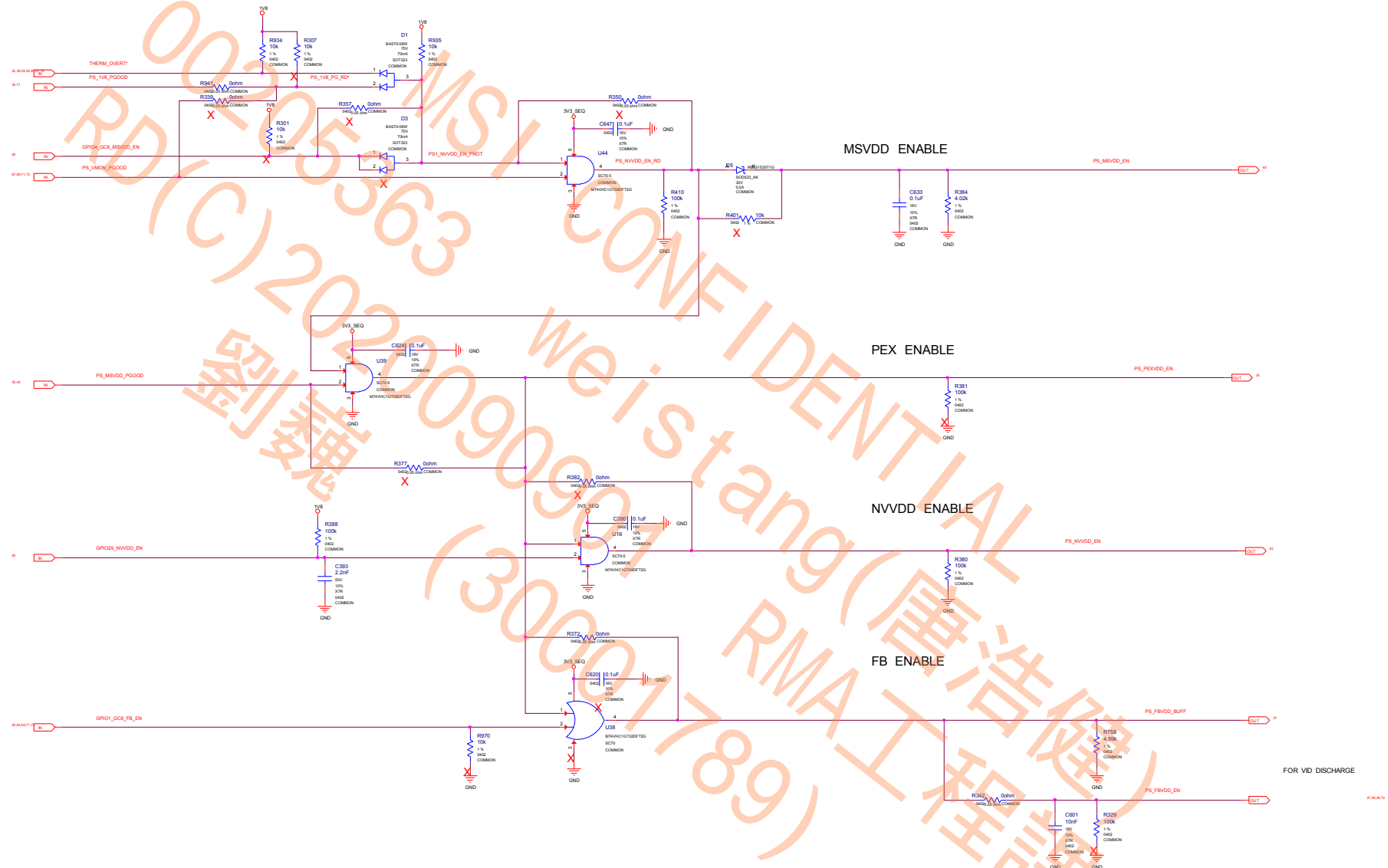
PS: Pre-Filter B



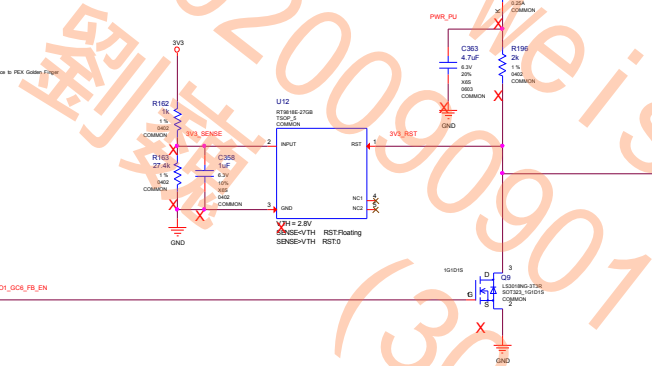
SEQUENCE:5V,1V8,3V3_SEQ ENABLE



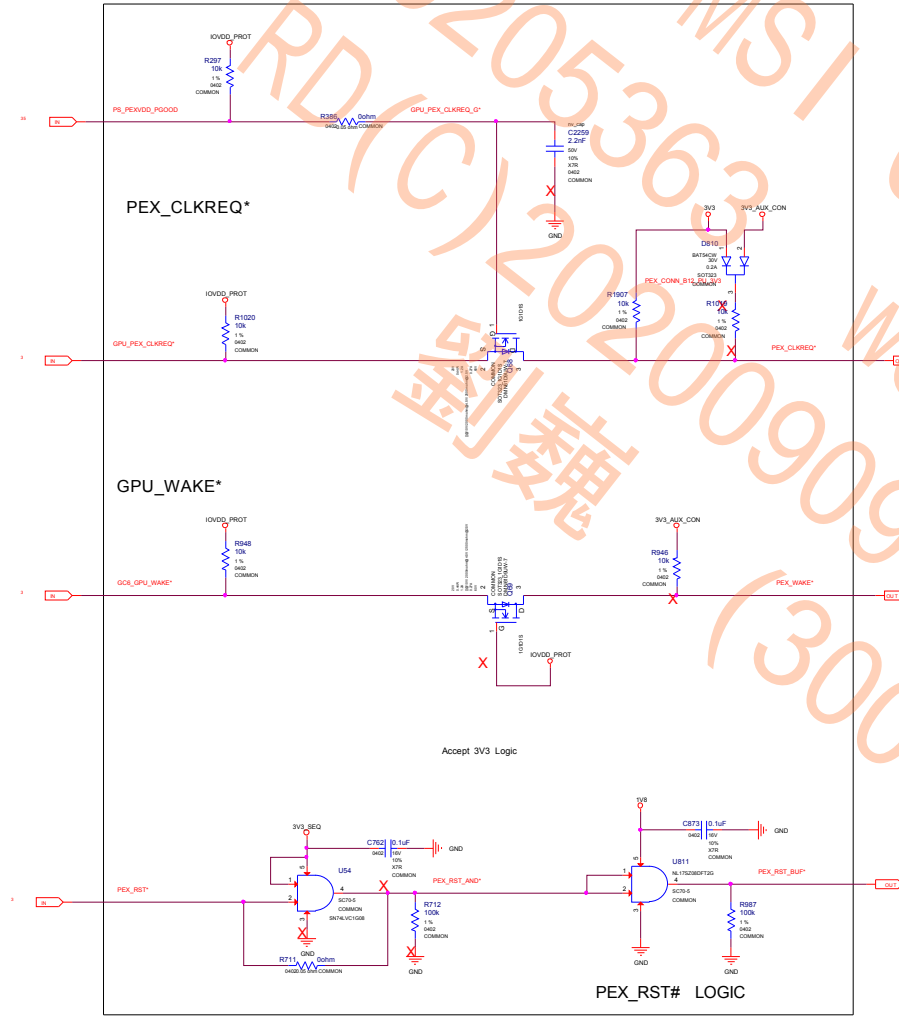
SEQUENCE:NV,PEX,FB ENABLE



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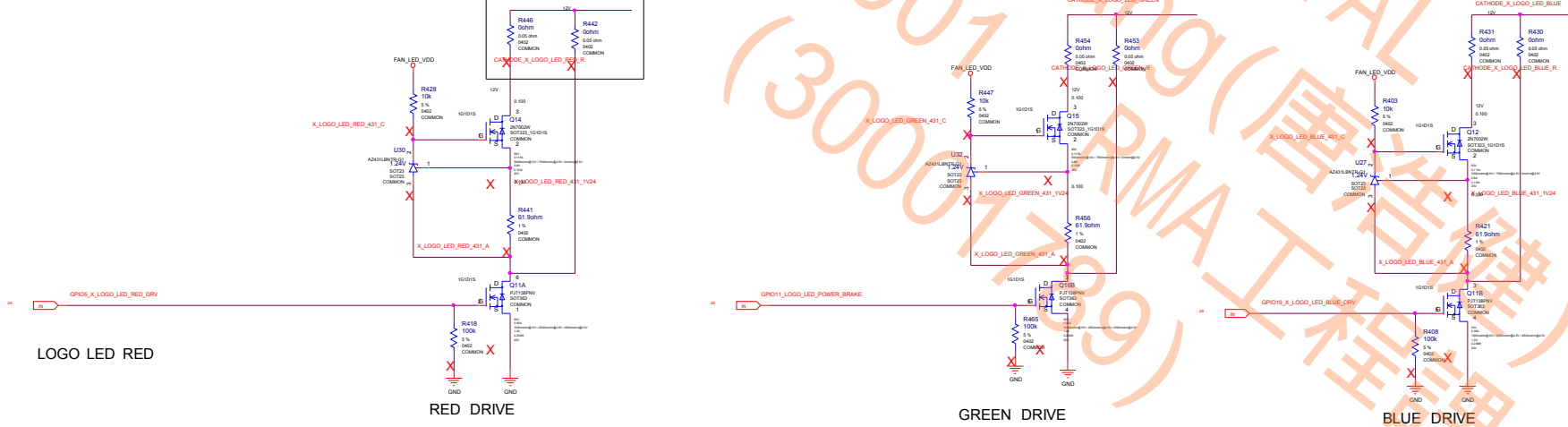
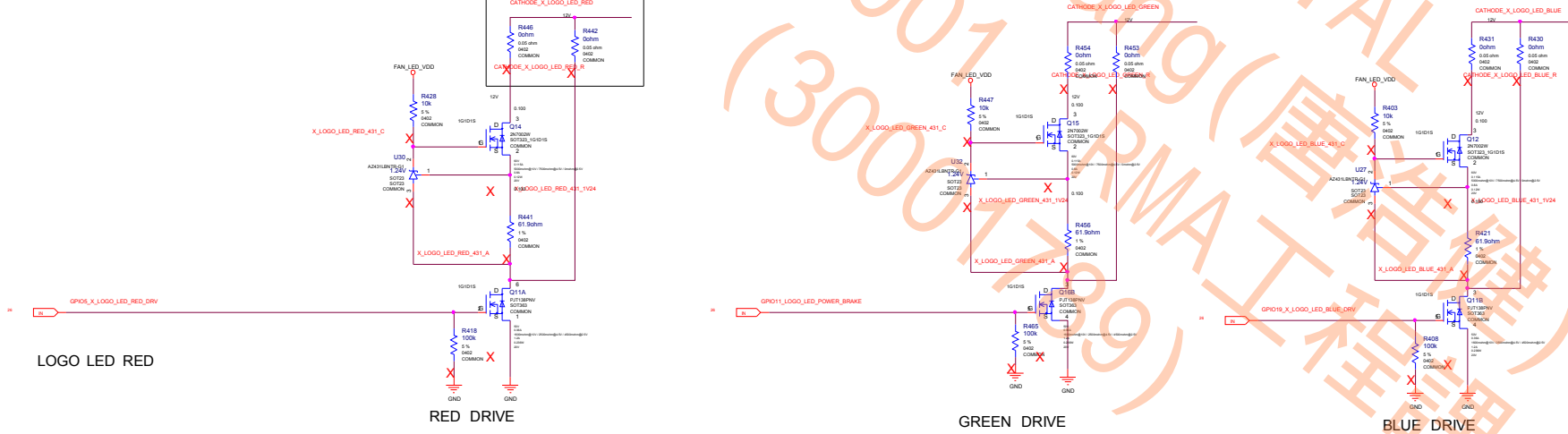
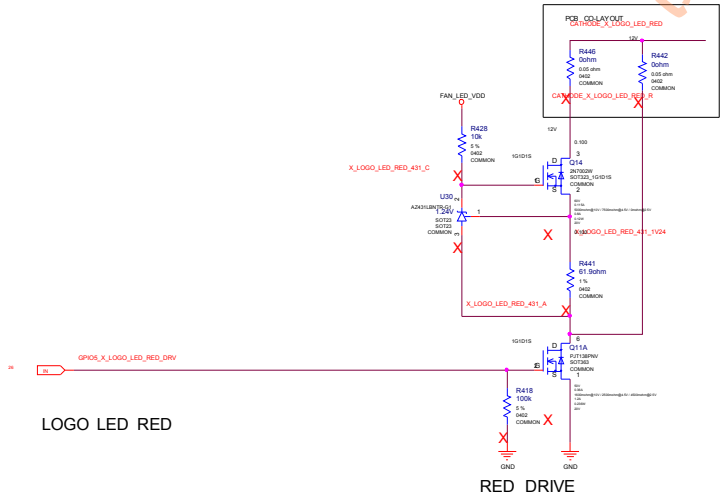
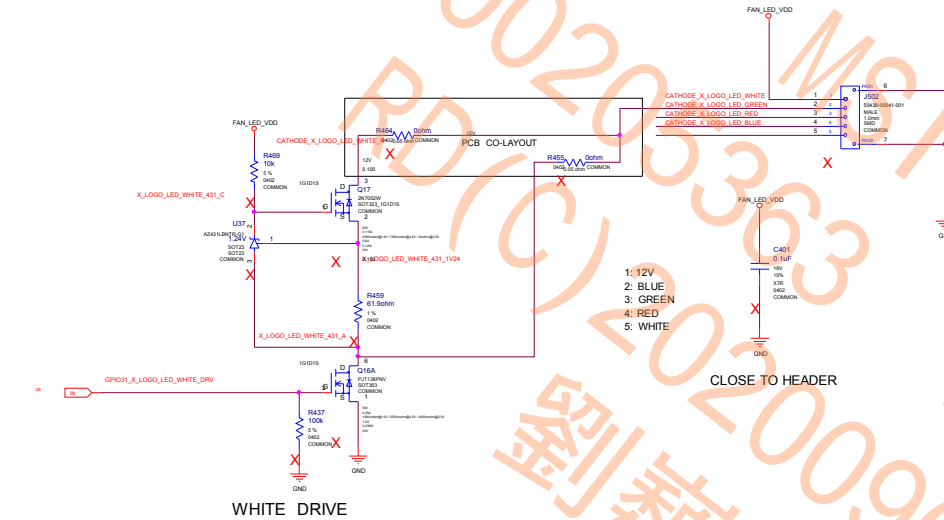
SEQUENCE:MISC



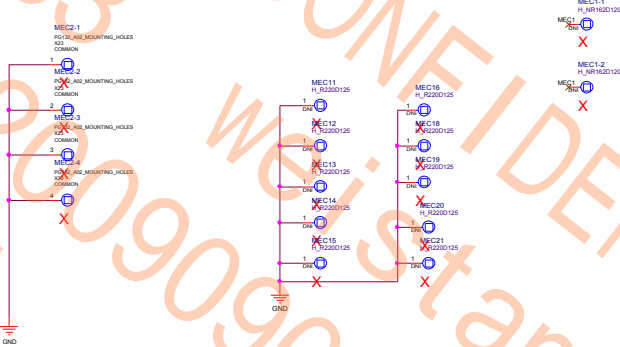
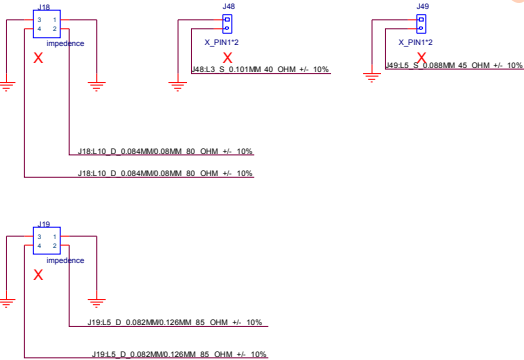
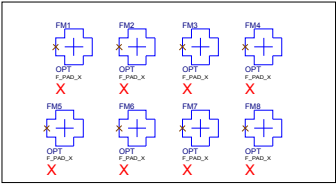


MISC: RGBW LED REF

CONNECTOR SIZE TO FIT LAYOUT
ALL CIRCUIT NO STUFF BY DEFAULT
ALIGN WITH PASH
IF ADDITIONAL POWER CONSUMPTION R
NEEDED, IT SHOULD BE ON LED MOD.

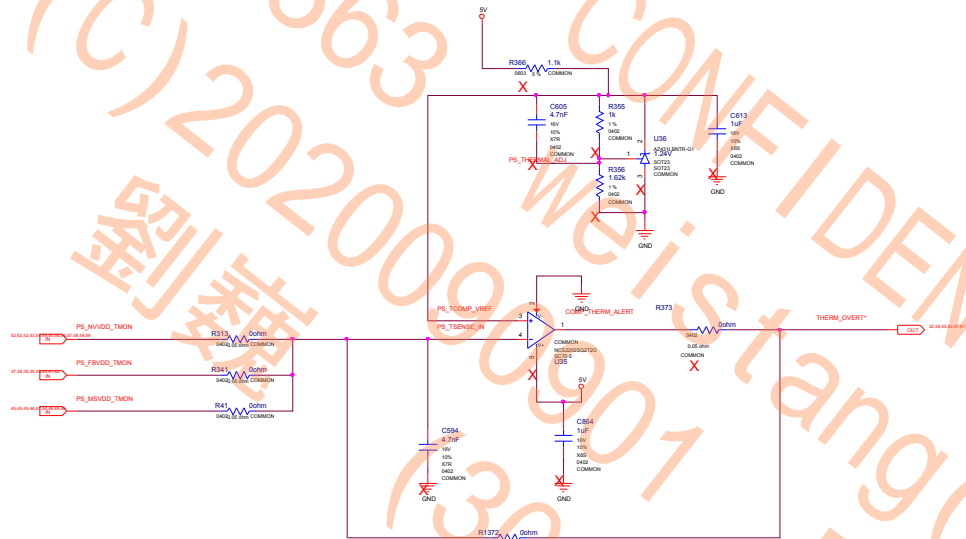


Mechanical: Mounting holes



The schematic diagram illustrates the internal components of the PS-TH1000-20T power supply module. Key components include:

- Input Section:** A 5V input connected to a 1k resistor (R355) and a 4.7nF capacitor (C605) to ground. The input signal is connected to the gate of the MOSFET (Q1).
- Switching Section:** The MOSFET (Q1) is connected to the output filter inductor (L1) and the output capacitor (C613).
- Output Section:** The output is connected to the output terminal (OUT) through a 0.1uF capacitor (C613) and a 1k resistor (R373).
- Feedback Section:** The feedback network consists of resistors R313, R343, and R41, which are connected to the feedback pin (FB) of the MOSFET driver.
- Thermal Protection:** A thermal protection circuit is shown, including a thermal alert pin (THERM_ALERT) and a thermal overvoltage pin (THERM_OVRT).
- Other Components:** The diagram also shows various capacitors (C605, C613, C604, C606) and resistors (R355, R313, R343, R41, R373) used for filtering and timing.



PCI TERM

